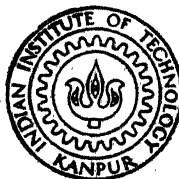


# STABILITY, POWER GAIN AND PORT- IMMITTANCES OF LINEAR ACTIVE TWO-PORT NETWORKS

BY

PINGALI SATYANJANEYA SARMA



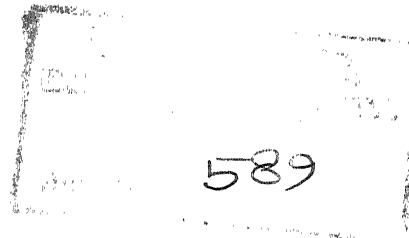
DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

JANUARY, 1971

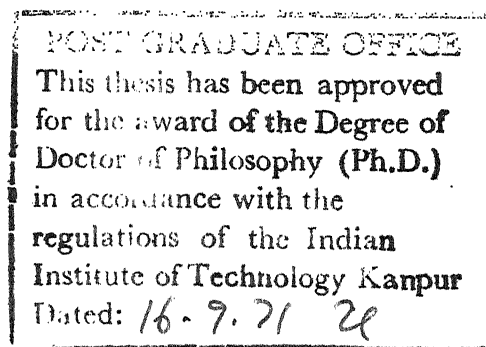
# STABILITY, POWER GAIN AND PORT- IMMITTANCES OF LINEAR ACTIVE TWO-PORT NETWORKS

A Thesis Submitted  
In Partial Fulfilment of the Requirements  
for the Degree of  
DOCTOR OF PHILOSOPHY



BY

PINGALI SATYANJANEYA SARMA



*Thesis  
621.3102  
Sarma*

to the

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

JANUARY, 1971

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TO

MY

BROTHER

VENKATA SIVARAMA KRISHNAYYA

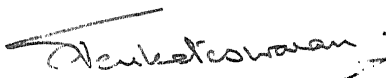
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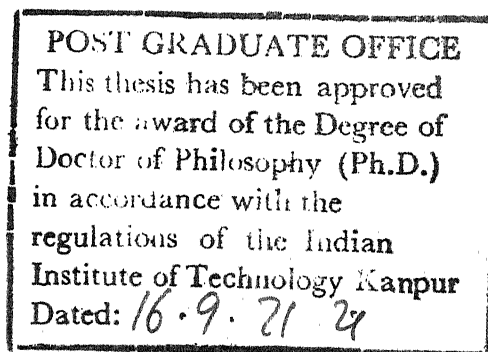
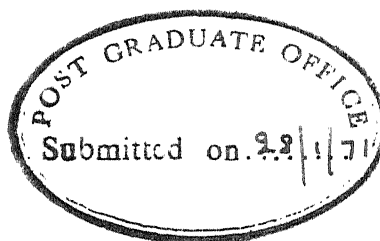
WITH RESPECT

CERTIFICATE

Certified that this work on STABILITY, POWER GAIN  
AND PORT IMMITTANCES OF LINEAR ACTIVE TWO-PORT NETWORKS , has  
been carried out under my supervision and has not been submitted  
elsewhere for a degree.

  
(S. Venkateswaran)  
Professor

Department of Electrical Engineering  
Indian Institute of Technology Kanpur



## ACKNOWLEDGEMENTS

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P. S. Sarma

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## LIST OF SYMBOLS, ABBREVIATIONS AND SUFFIXES

### Symbols:

The page number refers to the page on which the symbol appears first.

$a_1, b_1$	Centre coordinates of input reactance circles, p.21.
$a_2, b_2$	Centre coordinates of output reactance circle, p.22.
$A_1, B_1$	Centre coordinates of input resistance circle, p.23.
$A_2, B_2$	Centre coordinates of output resistance circle, p.23.
$b$	$\text{Im}(y)$ , p. 40.
$b_o$	Output susceptance, p. 40.
$b_s$	$\text{Im}(y_{12} + y_{21})$ , p. 45.
$b_S$	Terminating susceptance at the input port, p. 42.
$c_1$	Radius of input reactance circle, p. 21.
$c_2$	Radius of output reactance circle, p. 22.
$C_1$	Radius of input resistance circle, p. 23.
$C_2$	Radius of output resistance circle, p. 23.
$C'$	Centre of the circle, p. 24.
$g$	$\text{Re}(y)$ , p. 40.
$g_o$	Output conductance, p. 40.
$g_s$	$\text{Re}(y_{12} + y_{21})$ , p. 45.
$g_S$	Terminating conductance at the input port, p. 56.
$G_A$	Available power gain, p. 12.
$G_P$	Power gain, p. 12.
$G_T$	Transducer power gain, p. 12.

$k$	Stern's stability factor, p. 9.
$k_i$	Stern's inherent stability factor, p. 9.
$K$	Sensitivity of total port immittance to small immittance changes in the total self immittance at the opposite port, p. 30.
$K'$	Sensitivity as above but for large reactive changes, p. 33.
$K''$	Sensitivity as above but for large resistive changes, p. 34.
$L$	$ p_{12} p_{21} $ where $p$ is $h$ -, $z$ -, $y$ - or $g$ -, p. 6.
$L_o$	Inductance, p. 49.
$M$	$\text{Re} (p_{12} p_{21})$ , p. 6.
$N$	$\text{Im} (p_{12} p_{21})$ , p. 6.
$O$	Origin of axes of complex plane, p. 8.
$O'$	New origin ( $\rho_{11}$ , $\sigma_{11}$ ), p. 24.
$\begin{bmatrix} p_{11} & p_{12} \\ p_{21} & p_{22} \end{bmatrix}$	General two-port matrix where $p = h, z, y, \text{ or } g$ , p.5.
$p_1$ and $p_2$	Total self immittance of input and output port, p.6.
$p_{in}$	Input immittance, p. 5.
$p_{out}$	Output immittance, p. 5.
$p_L$	Load immittance, p. 5.
$p_S$	Source immittance, p.5.
$p_{p_1}$ and $p_{p_2}$	Total port immittance at input and output ports, p.14.
$p_{O1}, p_{O2}$	Image matching termination for device network at input and output port, p. 16.

[P]	General matrix of two-port modified by reactive paddings, p. 16.
$P_{avo}$	Power available at the output port, p. 11.
$P_{avs}$	Power available from the source, p. 11.
$P_i$	Power into the two-port, p. 11.
$P_o$	Power supplied to the load, p. 11.
$P_{01}$ and $P_{02}$	Input and output image matching terminations for the modified network, p. 17.
Q	Quality factor of inductor, p. 36.
$r_b$	Base resistance of transistor, p. 52.
$r_{b'}$	Base spreading resistance of transistor, p. 37.
$r_c$	Collector resistance of transistor, p. 52.
$r_e$	Emitter resistance of transistor, p. 37.
s	Invariant stability factor, p. 10.
$s_i$	Invariant inherent stability factor, p. 10.
$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$	Short circuit admittance matrix, p. 40.
$y_s$	$(y_{12} + y_{12})$ , p. 45.
$\theta$	Phase angle of $(p_{12} \ p_{21})$ , p. 6.
$\theta_1$	Phase angle of $(p_{11} + j\sigma_S)$ , p. 17.
$\theta_2$	Phase angle of $(p_{22} + j\sigma_L)$ , p. 17.
$\theta_3$	Phase angle of $\{(p_{11} + j\sigma_S)(p_{22} + j\sigma_L) - p_{12} \ p_{21}\}$ , p. 1
$\alpha$	Common base current gain, p. 50.
$\alpha_o$	Common base low frequency current gain, p. 37.
$\beta$	Common emitter current gain, p. 37.

$\beta_o$	Common emitter low frequency current gain, p. 38.
$\rho$	Re (p), p. 6.
$\rho_{in}$	Re ( $p_{in}$ ), p. 6.
$\rho'_{in}$	( $\rho_{in} - \rho_{11}$ ) new real axis, p. 24.
$\sigma$	Im (p), p. 6.
$\sigma_{in}$	Im ( $p_{in}$ ), p. 14.
$\sigma'_{in}$	( $\sigma_{in} - \sigma_{11}$ ) new imaginary axis, p. 24.
$\omega$	Angular frequency, p. 8.
$\eta$	Invariant factor, p. 10.
$\eta_i$	Inherent invariant factor, p. 10.
$\delta$	( $\eta - 1$ )/2. Inverse of sensitivity modulus maximum, p. 3.
$\Delta$	( $y_{11} y_{22} - y_{12} y_{21}$ ), p. 45.
$\Delta_r$	Re ( $\Delta$ ), p. 45.
$\Delta_i$	Im ( $\Delta$ ), p. 45.

#### Abbreviations:

Dr	Denominator, p. 6.
MAG	Maximum available power gain, p. 10.
Nr	Numerator, p. 6.

#### Suffixes:

S	Source termination.
L	Load termination.
opt	Optimum termination.

## SYNOPSIS

STABILITY, POWER GAIN AND PORT  
IMMITTANCES OF LINEAR ACTIVE  
TWO-PORT NETWORKS  
A Thesis Submitted  
In Partial Fulfilment of the Requirements  
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PINGALI SATYANJANEYA SARMA  
to the  
Department of Electrical Engineering  
Indian Institute of Technology Kanpur  
January 1971.

When one varies the source and load reactances during tuning of RF and IF amplifiers oscillations usually occur. This is due to the feedback within the device. Sufficient energy is fed back at the input terminal to cause oscillations. Feedback also makes the input immittance a function of the load immittance and the output immittance a function of source immittance. The device may be represented as a nonunilateral active two-port network and a black box approach can be adopted for the analysis of these problems.

Stern proposed a stability factor,  $k$ , in terms of the two-port parameters. For the two-port to be absolutely stable his stability factor  $k \geq 1$ . Venkateswaran proposed another stability factor,  $s$ , which unlike Stern's stability factor is an invariant in  $h$ -,  $z$ -,  $y$ - and  $g$ - matrix environments. Provided  $s \geq 1$ , he showed that this stability factor and the maximum available power gain are simply related through the loop gain modulus. He also proposed an alignability factor,  $\delta$ , which is

an invariant in the four matrix environments. This factor specifies the maximum interaction between ports.

In the present work, it is shown (without evaluating the optimum terminations) that conjugate matching passive terminations provide the maximum power gain for a given absolutely stable two-port network. These optimum terminations are derived based on a simple application of the well known image parameter theory.

A practical method is presented for quickly computing the 'invariant stability factor', optimum terminations and maximum available power gain from eight simple measurements.

A detailed study is carried out on the variation of port immittances for various terminating immittances at the opposite port. It is shown that the locus of port immittance is a circle for purely real terminations at the opposite port. Expressions are given for evaluating the load for a given input immittance on this circle. Sensitivity or interaction between ports is also investigated.

These results are used to obtain a design procedure for high  $Q$  inductive reactance from the circuits of Jindal and Dutta Roy. This design procedure is in terms of two-port admittance matrix parameters.

## CHAPTER 1

### INTRODUCTION

Linear active networks, in particular linear active two-port networks forms an important branch of electronics. It has received considerable attention with the invention of the transistor. Even nonlinear circuits like oscillators and mixers have been investigated under this head as it is simpler to apply linear analysis to network problems.

Investigators in the area of linear active two-port networks were mainly concerned with the problem of stability, power gain and sensitivity as they have a bearing on the performance of the basic (electronic) amplifier.

Linville<sup>1</sup> (1955), Stern<sup>3</sup> (1956), Bahrs<sup>4</sup> (1957), Venkateswaran and Booth Royd<sup>15</sup> (1960), and several others investigated the problem of stability and maximum available power gain of active two-ports. Works of Stern and Bahrs are on similar lines though carried out independently.

Stern<sup>3</sup> derived the conditions for the stability of two-ports in terms of its parameters and proposed a stability factor. His approach to the problem was from port immittances. For stability the port immittance should have a non negative real part for any passive termination at the opposite port.

Venkateswaran<sup>16</sup> (1961) proposed another stability factor which is an invariant in h-, z-, y- and g- matrix environments. He also showed that the maximum available power gain of an active two-port is simply related to this 'invariant stability factor'.

Investigations of Linvill<sup>1</sup> and others reveal that the two-port can deliver maximum power only when it is provided with conjugate matched source and load terminations. They first derived these terminations and later showed that they are conjugate matched terminations of the active two-port.

The problem of maximum available power gain and associated terminations is investigated in Chapter 2. Without evaluating the port terminations, it is shown that the maximum power gain of an absolutely stable active two-port network is realisable with conjugate matching terminations. Later, the expressions for these terminations are obtained, based on a simple application of the well known image parameter theory.

A practical method is presented in Chapter 3 for quickly computing Venkateswaran's invariant stability factor, optimum source and load terminations and maximum available power gain. This is an extension of Zawels<sup>25</sup> (1963) method.

Zawels showed that the locus of the port immittance is a circle for purely lossless terminations at the opposite port. The locus of port immittance for purely real terminations, the

termination required for any point on the immittance circle and the axis of skew symmetry are investigated in Chapter 3.

Venkateswaran<sup>29</sup> (1968) investigated the maximum interaction between port immittances for small immittance changes and large reactance (susceptance) changes at one of these ports. An 'invariant alignability factor' was obtained from the maximum interaction.

In Chapter 3 an exact expression for the interaction between port immittances is obtained for small immittance changes at a port. The maximum interaction between ports is also investigated for large resistance (conductance) changes of terminating immittance. These interactions expressed as sensitivity measure are shown to be related to the centres and radii of input and output port immittance circles.

The port immittance circle can be shifted in the complex plane by proper feedback and termination. This suggested a possible application in the analysis and design of active R-C circuits realising inductive reactance.

Introduction of integrated circuits created the problem of realising driving point inductive reactance with active semiconductor devices and R-C elements. Jindal<sup>34</sup> (1967) and Dutta Roy<sup>44</sup> (1964) reported circuits which can realise inductive reactance with high or even infinite Q. Analysis and design of these circuits is presented in Chapters 4 and 5. This is in terms of short circuit admittance matrix parameters.

## CHAPTER 2

### STABILITY AND POWER GAIN

#### 2.1 Stability:

##### 2.1.1 Introduction:

A non unilateral active two-port network can become unstable in the absence of external feedback provided that suitable terminations are connected to its terminal pairs.<sup>1-7</sup> Instability may be desirable, as in the case of oscillator circuits.<sup>8</sup> In many other applications, however, the network containing an active element is expected to be stable.

The stability of any given network can be analysed by locating its poles and zeros in the complex plane.<sup>9</sup> It is, however, often useful and simpler to formulate the question of stability in the following, rather general, manner. "What is the range of terminating immittance values at terminal pair 1/pair 2 and what is the frequency range for which the active element exhibits instability, if suitably terminated at terminal pair 2/pair 1?"<sup>3</sup>

This question can be answered by analysing the properties of the driving point immittances of the active two-port under different conditions of termination. Potential (not necessarily actual) instability exists if the real component of the driving immittance becomes negative at some real frequency.<sup>3</sup>

### 2.1.2 Potential Instability and Absolute Stability:

If the internal feedback within an active two-port is sufficient to support oscillations that device is said to be potentially unstable. This statement may be clarified by reference to Figure 2.1. If there can be found some combination of source immittance  $p_S$  and load immittance  $p_L$  that will cause oscillations, the active two-port in Figure 2.1 is potentially unstable. On the otherhand, if no combination of passive terminations can cause oscillations, the two-port is said to be absolutely stable. The conditions

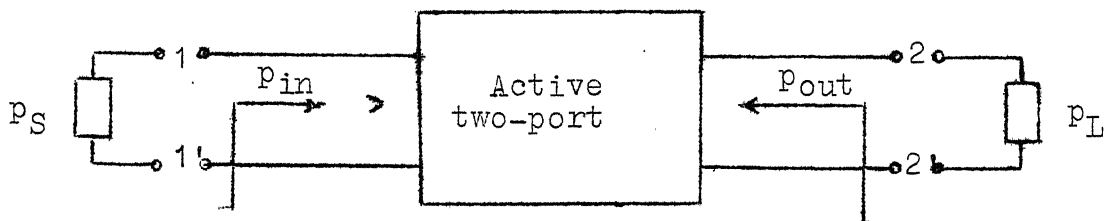


Fig. 2.1: An active two-port with source and load terminations.

for absolute stability in terms of general active two-port matrix parameters are derived below.

### 2.1.3 Conditions for Absolute Stability:

Characterise the two-port represented in Figure 2.1, by its general matrix

$$\begin{bmatrix} p_{11} & p_{12} \\ p_{21} & p_{22} \end{bmatrix} \quad \dots \quad (2.1)$$

where  $p_{11}$  etc. may be sets of h-, z-, y-, or g- matrix parameters.  $p_S$  and  $p_L$  are its passive source and load immittances,  $p_{in}$  and  $p_{out}$  are the driving point immittances of the input and output ports respectively.

For a two-port to be absolutely stable, the input and output port driving point immittances must have a non-negative real part for all passive terminations. If this condition is violated at any frequency, the active two-port is potentially unstable.<sup>3</sup>

The load immittance  $p_L$  that minimizes the real part of  $p_{in}$  is obtained. Then the minimum value of this real part will be calculated, and the conditions under which this minimum is greater than zero will be determined. Similar analysis holds for the output port immittance where the source immittance  $p_S$  is varied.

The input port immittance  $p_{in}$  is given by

$$p_{in} = p_{11} - \frac{p_{12} p_{21}}{p_{22} + p_L} \quad \dots(2.2)$$

Let  $p_{12} p_{21} = M + jN = L \angle \theta$ ,  $p_{22} + p_L = p_2$ ,  $p_{11} + p_S = p_1$ ,  $p_{lm} = \rho_{lm} + j\sigma_{lm}$  and  $p_x = \rho_x + j\sigma_x$  ... (2.3)

Then,

$$\rho_{in} = \text{Real}(p_{in}) = \rho_{11} - \frac{M(\rho_{22} + \rho_L) + N(\sigma_{22} + \sigma_L)}{(\rho_{22} + \rho_L)^2 + (\sigma_{22} + \sigma_L)^2} \quad \dots(2.4)$$

$$= \frac{(\rho_{22} + \rho_L)^2 + (\sigma_{22} + \sigma_L)^2 - \frac{M}{\rho_{11}}(\rho_{22} + \rho_L) - \frac{N}{\rho_{11}}(\sigma_{22} + \sigma_L)}{\frac{1}{\rho_{11}} \{ (\rho_{22} + \rho_L)^2 + (\sigma_{22} + \sigma_L)^2 \}} \quad \dots(2.5)$$

$$= \frac{Nr}{Dr} \quad \dots(2.6)$$

$\rho_{11} > 0$  for the network to be short circuit/open circuit stable. Therefore, in order to examine the non negative values of  $\rho_{in}$ , one need only consider the sign of numerator. Numerator Nr may be rewritten as

$$\begin{aligned} \text{Nr} = \left\{ \rho_L + \left( \rho_{22} - \frac{M}{2\rho_{11}} \right) \right\}^2 + \left\{ \sigma_L + \left( \sigma_{22} - \frac{N}{2\rho_{11}} \right) \right\}^2 \\ - \frac{L^2}{4\rho_{11}^2} \end{aligned} \quad \dots(2.7)$$

Therefore

$$\left( \text{Nr} + \frac{L^2}{4\rho_{11}^2} \right) = \left\{ \rho_L + \left( \rho_{22} - \frac{M}{2\rho_{11}} \right) \right\}^2 + \left\{ \sigma_L + \left( \sigma_{22} - \frac{N}{2\rho_{11}} \right) \right\}^2 \quad \dots(2.8)$$

after making use of Eqn. (2.3). Eqn. (2.8) represents a family of concentric circles with Nr as the parameter, with a common centre  $\left\{ \left( \frac{M}{2\rho_{11}} - \rho_{22} \right), \left( \frac{N}{2\rho_{11}} - \sigma_{22} \right) \right\}$  in the  $(\rho_L, \sigma_L)$  plane as shown in Figure 2.2(a).<sup>3</sup> The radius varies from 0 to  $\infty$ , as Nr increases from  $-L^2/4\rho_{11}^2$  to  $\infty$ . The critical circle i.e., the circle for Nr = 0 is marked in the figure. All the inner circles correspond to Nr < 0 and the outer circles to Nr > 0. If Nr is to remain positive for any passive termination  $p_L$  which can be represented by a point  $(\rho_L, \sigma_L)$  in the right half plane (as  $\rho_L$  cannot be -ve) then, every point in the right half plane including the  $\sigma_L$ -axis must lie outside the critical circle. In other words the critical circle must be entirely in the left half plane.

Therefore,

$$\rho_{22} - \frac{M}{2\rho_{11}} > \frac{L}{2\rho_{11}} \quad \dots(2.9)$$

$$\text{or} \quad 2\rho_{11} \rho_{22} > L + M \quad \dots(2.10)$$

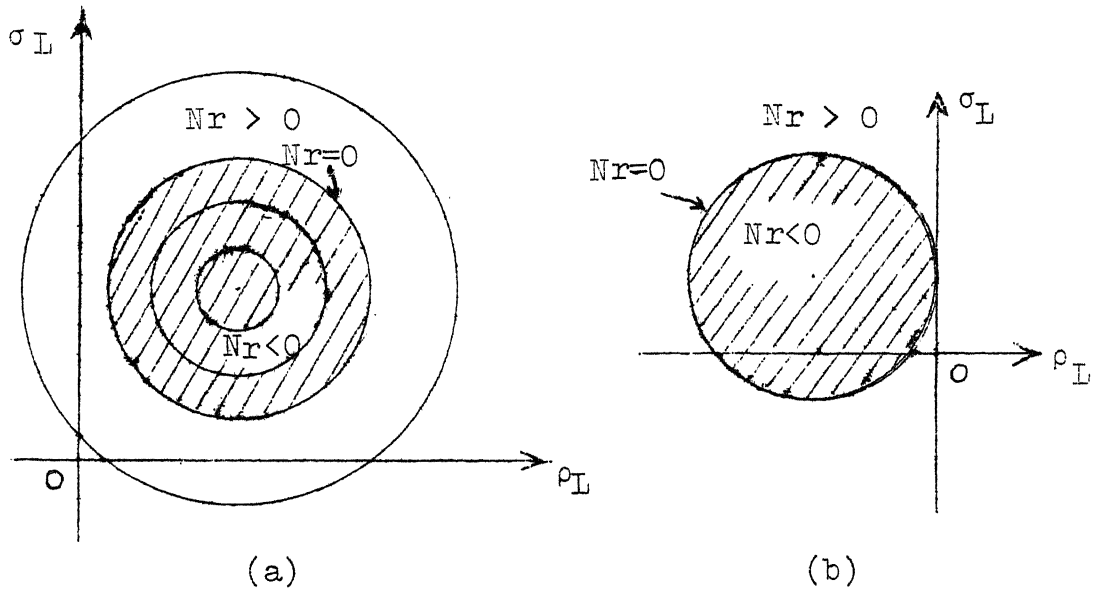


Fig. 2.2 (a) Family of concentric circles in  $(\rho_L, \sigma_L)$  plane with  $Nr$  as a parameter.

(b) Critical circle corresponding to  $Nr = 0$ .

Carrying out a similar analysis for the output port gives the same condition.

Hence, for the two-port to be absolutely stable for all  $\omega \geq 0$  the following conditions should be satisfied.<sup>3</sup>

$$\rho_{11} > 0 \quad \rho_{22} > 0 \quad \dots(2.11)$$

$$\text{and} \quad 2\rho_{11} \rho_{22} > L + M \quad \dots(2.12)$$

A potentially unstable two-port may be made absolutely stable by neutralization<sup>10-13</sup> or by loading the two-port with sufficiently large source and load conductances/resistances.<sup>14,15</sup>

#### 2.1.4 Stability Factors:

Based on the stability conditions given in Eqns. (2.11) and (2.12) Stern<sup>14</sup> defined a stability factor  $k$  as

$$k = \frac{2 \rho_1 \rho_2}{L + M} \quad \dots (2.13)$$

where  $\rho_1 = \rho_{11} + \rho_S$  and  $\rho_2 = \rho_{22} + \rho_L$ .

Thus  $k > 1$  for absolute stability with a given  $\rho_S$  and  $\rho_L$ . This is a stability factor of the two-port including  $\rho_S$  and  $\rho_L$ . An inherent stability factor  $k_i$  is defined by

$$k_i = \frac{2 \rho_{11} \rho_{22}}{L + M} \quad \dots (2.14)$$

Since  $\rho_1 \geq \rho_{11}$  and  $\rho_2 \geq \rho_{22}$

$$k \geq k_i \quad \dots (2.15)$$

Thus a two-port network which is potentially unstable ( $k_i \leq 1$ ) may be modified suitably so that the modified network is absolutely stable ( $k > 1$ ). The magnitude of stability factor  $k$  (or  $k_i$ ) depends upon the matrix used, and may be denoted by  $k_p$  where  $p = h, z, y, \text{ or } g$ . The magnitudes of  $k_p$  are all  $> 1$  or all  $= 1$  or all  $< 1$  in the regions of absolute stability, marginal stability, and potential instability respectively. Except in the case of marginal stability the values of  $k_p$  are different.<sup>15</sup>

Venkateswaran<sup>16</sup> defined another pair of factors called invariant factor  $\eta$  and inherent invariant factor  $\eta_i$  as follows:

$$\eta = \frac{2\rho_1\rho_2 - M}{L} \quad \dots (2.16)$$

$$\eta_i = \frac{2\rho_{11}\rho_{22} - M}{L} \quad \dots (2.17)$$

Unlike  $k$ , the invariant factor  $\eta$  is independent of the matrix used.

Venkateswaran<sup>16</sup> also define an invariant stability factor  $s$  by

$$s = \eta + \sqrt{(\eta^2 - 1)} \quad \dots (2.18)$$

Similarly, the inherent invariant stability factor  $s_i$  is defined by

$$s_i = \eta_i + \sqrt{(\eta_i^2 - 1)} \quad \dots (2.19)$$

For absolute stability of original and modified network respectively,

$$s_i > 1 \quad \dots (2.20)$$

$$\text{and } s > 1 \quad \dots (2.21)$$

As  $s_i$  (or  $s$ ) is function of  $\eta_i$  (or  $\eta$ ) alone, it is also independent of the matrix used. The stability factor  $s_i$  or  $s$  is simply related to MAG (the maximum available power gain) of an absolutely stable two-port network. The MAG is considered in the following sections.

## 2.2 Power Gain:

### 2.2.1 Introduction:

In an active two-port model (represented in Figure 2.3) which has infinite or zero input immittance, the amplification (ratio of output voltage or current to input voltage or current) is a very useful measure of performance. This is true, for example, in many vacuum tube circuits. However, for two-port networks which require power at the input port, as transistors do, it is frequently much more significant to measure performance in terms of the flow of power in the circuit.<sup>18</sup>

The power gain of an active two-port may be specified in many different ways, depending on operating conditions and the purpose for which the gain expression is derived. Three types of power gain expressions are commonly used. They are namely power gain  $G_P$ , transducer power gain  $G_T$  and available power gain  $G_A$ . These may be defined and expressed in terms of general matrix parameters with the help of Figure 2.3.<sup>19</sup>

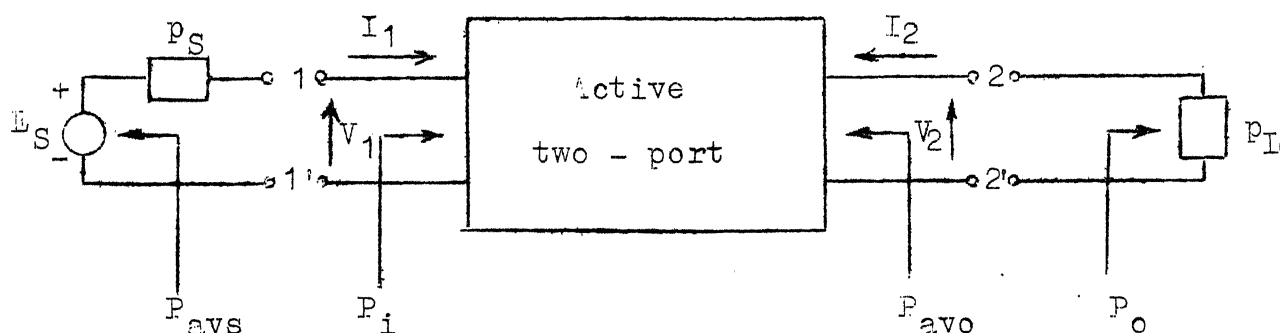


Fig. 2.3: General active two-port with source and load.

$$\begin{aligned}
 \text{Power gain } G_P &= \frac{\text{Power supplied to the load}}{\text{Power in to the two-port}} = \frac{P_o}{P_i} \\
 &= \left| \frac{p_{21}}{p_2} \right|^2 \frac{\rho_L}{\rho_{in}} \quad \dots (2.22)
 \end{aligned}$$

$$\begin{aligned}
 \text{Transducer power gain } G_T &= \frac{\text{Power delivered to the load}}{\text{Power available from the source}} = \frac{P_o}{P_{avs}} \\
 &= \frac{4 |p_{21}|^2 \rho_S \rho_L}{|p_1 p_2 - p_{12} p_{21}|^2} \quad \dots (2.23)
 \end{aligned}$$

$$\begin{aligned}
 \text{Available power gain } G_A &= \frac{\text{Power available at the output port}}{\text{Power available from the source}} = \frac{P_{avo}}{P_{avs}} \\
 &= \frac{|p_{21}|^2 \rho_S}{\text{Re} \{ (p_1 p_{22} - p_{12} p_{21}) p_1^* \}} \quad \dots (2.24)
 \end{aligned}$$

where Re stands for real part.  $p_1^*$  is the conjugate of  $p_1$ .

In general, there are no simple relationships among  $G_P$ ,  $G_T$  and  $G_A$  because of the nature of their definitions. However, one simple relationship exists between  $G_P$ ,  $G_T$  and  $G_A$ , namely,  $(G_P)_{\max} = (G_T)_{\max} = (G_A)_{\max} = \text{MAG}$ ; provided that this maximum available power gain is finite; i.e., the two-port is absolutely stable.<sup>19</sup> Thus the maximum available power gain is unique and an important property of a two-port. Hence, it is of interest to find the conditions to be satisfied and the optimum terminations for maximum available power gain.

### 2.2.2 Maximum Available Power Gain:

To find the maximum available power gain and optimum terminations one may use any one of the following alternative methods:<sup>19</sup>

- (1) Maximize  $G_P$  with respect to the real and imaginary parts of the load immittance; then select the source impedance to conjugate match the input port terminated with  $(p_L)_{opt}$ .
- (2) Maximize  $G_T$  with respect to real and imaginary parts of the the source and load immittances.
- (3) Maximize  $G_A$  with respect to the real and imaginary parts of the source immittance, then select the load impedance to conjugate match the output port terminated with  $(p_S)_{opt}$ .

Several authors<sup>7,18-21</sup> studied the problem of maximum available power gain and optimum terminations required. The approach given below is simpler and probably more revealing than the methods available elsewhere.<sup>21</sup>

### 2.2.3 Types of Terminations for Maximum Available Power Gain:

The expression for transducer power gain  $G_T$ , of Eqn.(2.23) is rewritten below for convenience.

$$G_T = \frac{4|p_{21}|^2 \rho_S \rho_L}{|p_1 p_2 - p_{12} p_{21}|^2}$$

The denominator  $D_r$  in the expression for the transducer power gain can be rewritten as

$$D_r = (\rho_1 \rho_2 - \sigma_1 \sigma_2 - M)^2 + (\rho_1 \sigma_2 + \rho_2 \sigma_1 - N)^2 \quad \dots (2.25)$$

It can be observed that only the denominator contains  $\sigma_1$  and  $\sigma_2$ . Hence for a given  $\rho_1$  and  $\rho_2$ , we can maximize the power gain by minimizing the denominator.

Differentiate the denominator with respect to  $\sigma_1$  and  $\sigma_2$  and equate each differential coefficient to zero for maxima or minima of  $D_r$ , to get<sup>14,15</sup>

$$\frac{\sigma_1}{\rho_1} = \frac{\sigma_2}{\rho_2} = \lambda = \frac{\rho_1 \sigma_2 + \rho_2 \sigma_1 - N}{\rho_1 \rho_2 - \sigma_1 \sigma_2 - M} \quad \dots (2.26)$$

$$\text{or} \quad \rho_1 \rho_2 \lambda^3 + (\rho_1 \rho_2 + M) \lambda - N = 0 \quad \dots (2.27)$$

These conditions ensure<sup>22</sup> that

$$\sigma_{p_1} = \sigma_{in} + \sigma_S = 0 \text{ and } \sigma_{p_2} = \sigma_{out} + \sigma_L = 0 \quad \dots (2.28)$$

$$\text{where } p_{p_1} = p_1 - \frac{p_{12} p_{21}}{p_2} = \rho_{p_1} + j \sigma_{p_1}, \quad \dots (2.29)$$

$$p_{p_2} = p_2 - \frac{p_{12} p_{21}}{p_1} = \rho_{p_2} + j \sigma_{p_2}.$$

Hence for minimizing the denominator or maximizing the power gain, the imaginary part of the 'total port immittance' must vanish at each port. This is true for all values of  $\rho_1$  and  $\rho_2$ .

The power gain expression can be rewritten as

$$G_T = \frac{4 |p_{21}|^2 \rho_S \rho_L}{|p_2|^2 \left| p_1 - \frac{p_{12} p_{21}}{p_2} \right|^2} \quad \dots (2.30)$$

With reactances tuned out at the ports, power gain

$$G_T' = \frac{4|p_{21}|^2 \rho_S \rho_L}{|p_2|^2 \rho_{p_1}^2} \quad \text{or} \quad G_T' = \frac{|p_{21}|^2 \rho_L \cdot 4 \rho_{in} \rho_S}{|p_2|^2 \rho_{in} (\rho_{in} + \rho_S)^2} \quad (2.31)$$

since  $\rho_{p_1} = \rho_{in} + \rho_S$ . The factor  $\frac{4 \rho_{in} \rho_S}{(\rho_{in} + \rho_S)^2}$ , in the above expression has a maximum value of unity when  $\rho_{in} = \rho_S$  so that this maximum power gain,

$$G_T'' = \frac{|p_{21}|^2 \rho_L}{|p_2|^2 \rho_{in}} \quad \dots \quad (2.32)$$

$G_T''$  can be maximized further with respect to  $\rho_L$  and  $\sigma_L$  to get the maximum available power gain. Similarly, it can be shown that power gain is a maximum for  $\rho_{out} = \rho_L$  to get  $G_T'''$  which can be maximised further with respect to  $\rho_S$  and  $\sigma_S$  to get the same maximum available power gain as above. To realise this unique maximum available power gain, the conditions

$$\rho_S = \rho_{in} \quad \text{and} \quad \rho_L = \rho_{out} \quad \dots \quad (2.33)$$

should be simultaneously satisfied in addition to the stipulation  $\sigma_{p_1} = \sigma_{p_2} = 0$ .

Hence, for the maximum available power gain the following four conditions should be satisfied:<sup>21</sup>

$$\sigma_S = -\sigma_{in}, \quad \sigma_L = -\sigma_{out}, \quad \rho_S = \rho_{in} \quad \text{and} \quad \rho_L = \rho_{out} \quad (2.34)$$

Clearly these four stipulations ensure conjugate matching terminations for the given active two-port network and realise its maximum available power gain.

#### 2.2.4 Optimum Terminations and Maximum Available Power Gain:

It is now established that conjugate matching terminations give the maximum available power gain for the active two-port network. Expressions for these terminations will be derived based on the well known image parameter theory.<sup>23,24</sup>

Consider a device network with a general matrix  $[p]$ . Add a lossless source immittance and lossless load immittance  $j\sigma_S$  and  $j\sigma_L$  respectively to produce a modified network as in Figure 2.4. This modified network is representable by its general matrix

$$[P] = \begin{bmatrix} P_{11} & P_{12} \\ P_{21} & P_{22} \end{bmatrix} \quad \dots \quad (2.35)$$

Let its image matching terminations<sup>23</sup> be real i.e.  $P_{01} = \rho_{01}$  and  $P_{02} = \rho_{02}$ . Hence, for this modified network, image matching and conjugate matching terminations are identical. Terminations  $j\sigma_S$  and  $j\sigma_L$  must be such as to make the two image immittances purely real. Thus  $\sigma_{p_1} = \sigma_{p_2} = 0$  for the modified network with source and load terminations,  $P_{01} = \rho_{01} = \rho_S$  and  $P_{02} = \rho_{02} = \rho_L$  respectively. Therefore, for the original device network,  $\rho_S + j\sigma_S$  and  $\rho_L + j\sigma_L$  are conjugate matching immittances.

For the device network<sup>23</sup>

$$\begin{aligned} \rho_{01} &= \sqrt{\frac{P_{11}}{P_{22}}} (P_{11} P_{22} - P_{12} P_{21}) \\ \text{and} \quad \rho_{02} &= \sqrt{\frac{P_{22}}{P_{11}}} (P_{11} P_{22} - P_{12} P_{21}) \end{aligned} \quad \dots \quad (2.36)$$

For the modified network

$$P_{01} = \sqrt{\left[ \frac{p_{11} + j\sigma_S}{p_{22} + j\sigma_L} \right] \left\{ (p_{11} + j\sigma_S)(p_{22} + j\sigma_L) - p_{12} p_{21} \right\}}$$

and

$$P_{02} = \sqrt{\left[ \frac{p_{22} + j\sigma_L}{p_{11} + j\sigma_S} \right] \left\{ (p_{11} + j\sigma_S)(p_{22} + j\sigma_L) - p_{12} p_{21} \right\}}$$

... (2.37)

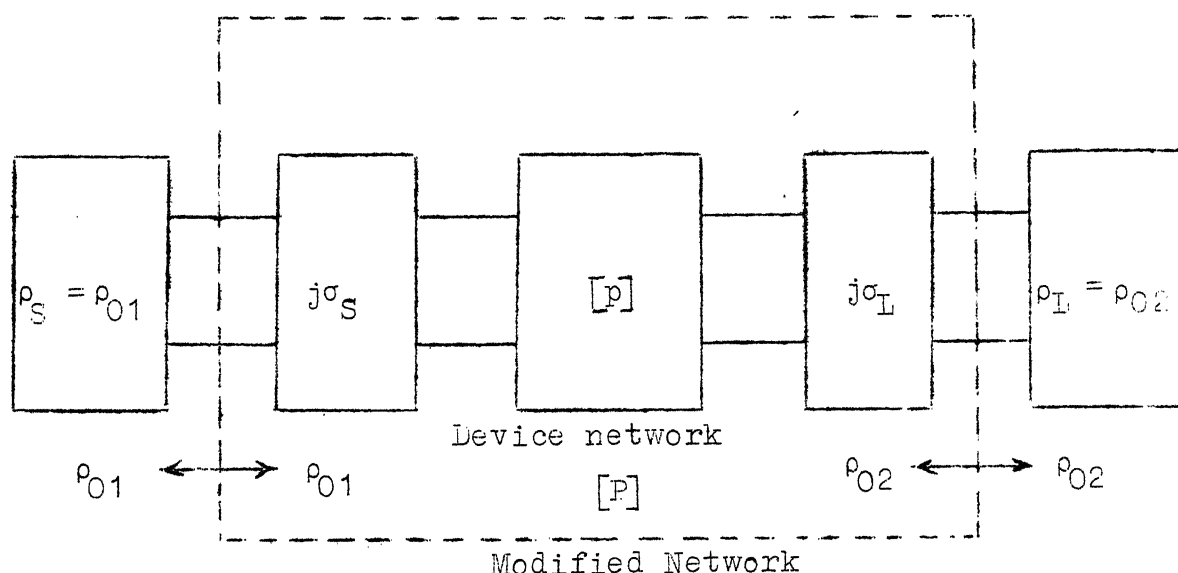


Fig. 2.4: 'Device Network' modified by reactive paddings such that the 'modified network' has purely real image matching parameters.

Phase angle of  $P_{01} = (\theta_1 - \theta_2 + \theta_3)/2$  and phase angle of  $P_{02} = (\theta_2 - \theta_1 + \theta_3)/2$  where  $\theta_1$ ,  $\theta_2$  and  $\theta_3$  refer to the phase angles of  $(p_{11} + j\sigma_S)$ ,  $(p_{22} + j\sigma_L)$  and  $\{(p_{11} + j\sigma_S)(p_{22} + j\sigma_L) - p_{12} p_{21}\}$  respectively.

$$\theta_1 - \theta_2 + \theta_3 = \theta_2 - \theta_1 + \theta_3 = 0 \quad \dots (2.38)$$

as  $P_{01}$  and  $P_{02}$  are constrained to be real. Hence

$$\theta_1 = \theta_2 \quad \text{and} \quad \theta_3 = 0. \quad \dots \quad (2.39)$$

From these conditions it simply follows that

$$\frac{\sigma_{11} + \sigma_S}{\rho_{11}} = \frac{\sigma_{22} + \sigma_L}{\rho_{22}} \quad \dots \quad (2.40)$$

$$\text{and} \quad \rho_{11} (\sigma_{22} + \sigma_L) + \rho_{22} (\sigma_{11} + \sigma_S) - N = 0$$

$$\text{or} \quad 2\rho_{11} (\sigma_{22} + \sigma_L) - N = 0 \quad \dots \quad (2.41)$$

This gives

$$\sigma_S = -\sigma_{11} + \frac{N}{2\rho_{22}}, \quad \sigma_L = -\sigma_{22} + \frac{N}{2\rho_{11}} \quad \dots \quad (2.42)$$

$$\text{and} \quad (p_{11} + j\sigma_S)(p_{22} + j\sigma_L) - p_{12}p_{21} = \rho_{11}\rho_{22} - M - \frac{N^2}{4\rho_{11}\rho_{22}} \quad \dots \quad (2.43)$$

$$\begin{aligned} \text{Hence} \quad P_{01} = \rho_{01} = \rho_S &= \rho_{11} \sqrt{1 - \frac{M}{\rho_{11}\rho_{22}} - \frac{N^2}{4\rho_{11}^2\rho_{22}^2}} \\ &= \frac{L}{2\rho_{22}} \sqrt{(\eta_i^2 - 1)} \quad \dots \quad (2.44) \end{aligned}$$

Similarly,

$$P_{02} = \rho_{02} = \rho_L = \frac{L}{2\rho_{11}} \sqrt{(\eta_i^2 - 1)} \quad \dots \quad (2.45)$$

where  $L = |p_{12}p_{21}|$  and the 'inherent invariant factor',<sup>16</sup>

$$\eta_i = \frac{2\rho_{11}\rho_{22} - M}{L} \quad \text{as defined in Ecn. (2.17).}$$

The maximum available power gain of an active two-port network is obtainable from the above conjugate matching terminations. It is given by<sup>16</sup>

$$\text{MAG} = \left| \frac{p_{21}}{p_{12}} \right| \frac{1}{\eta_i + \sqrt{(\eta_i^2 - 1)}} = \frac{1}{s_i} \left| \frac{p_{21}}{p_{12}} \right| \dots \quad (2.46)$$

where  $s_i$  is the 'inherent invariant stability factor' defined in Eqn. (2.19).

Having realised the importance of stability factor and its relation to power gain one would like to evaluate these important factors for a given two-port. One obvious method, of course, is to compute these quantities from the matrix parameters of the two-port. But the measurement of transfer parameters require special techniques or bridges. An easier and simpler method is available which depends upon the driving point immittances of the two-ports. This can be expected as the stability conditions are derived from the driving point immittances.

The driving point immittances are considered in the next chapter.

## CHAPTER 3

### PORT IMMITTANCES OF ACTIVE TWO-PORTS

#### 3.1 Introduction:

Locus of driving point immittance of input/output port of an active two-port network is a circle for lossless<sup>25-27</sup> or purely real (including -ve values) terminations. Termination required for any point on the circle can be obtained analytically or geometrically from the circle.<sup>28</sup>

The driving point immittance circles are useful tools in analysing active two-ports. The maximum modulus of sensitivity of the total port immittance to small immittance changes and large lossless immittance changes is an invariant.<sup>29</sup> The maximum modulus of sensitivity of the total port immittance to large purely real (including -ve values) immittance changes is also an invariant. The modulus of sensitivity is simply related to the coordinates of centres and radii of the immittance circles.

Invariant factor,<sup>16</sup>  $n$ , optimum real and imaginary parts of source and load immittances can be quickly computed from these circles<sup>27</sup>. Practical method of Cripps and Slatter<sup>30</sup> can be adopted for the measurement of 'measure of non-reciprocity',  $|\frac{p_{21}}{p_{12}}|$ , and the maximum available power gain can be computed from the relation<sup>16</sup>  $MAG = \frac{1}{S} |\frac{p_{21}}{p_{12}}|$ . Difficulties in the measurement of four-pole parameters with short and/or open circuits and tedious calculations are avoided by this.

### 3.2 Immittance Circles:

#### 3.2.1 Driving point Immittance of an Active Two-Port Terminated in Lossless Immittance:

Consider an active two-port terminated in a lossless immittance,  $j\sigma_L$ , at its output-port. Input port immittance of this two-port in terms of the general matrix parameters described in Eqn. (2.1) is given by

$$p_{in} = p_{11} - \frac{p_{12} p_{21}}{p_{22} + j\sigma_L} \quad \dots (3.1)$$

yielding

$$\rho_{in} = \rho_{11} - \frac{M\rho_{22} + N\sigma_2}{\rho_{22}^2 + \sigma_2^2} \quad \dots (3.2)$$

$$\text{and } \sigma_{in} = \sigma_{11} - \frac{N\rho_{22} - M\sigma_2}{\rho_{22}^2 + \sigma_2^2} \quad \dots (3.3)$$

where  $\sigma_2 = \sigma_{22} + \sigma_L$  and  $\rho_{11}$ ,  $\sigma_{11}$  etc. are defined by Eqn. (2.3).

Eliminate  $\sigma_2$  from Eqns. (3.2) and (3.3) to obtain

$$(\rho_{in} - a_1)^2 + (\sigma_{in} - b_1)^2 = c_1^2 \quad \dots (3.4)$$

$$\text{where } a_1 = \rho_{11} - \frac{M}{2\rho_{22}}, \quad b_1 = \sigma_{11} - \frac{N}{2\rho_{22}} \text{ and } c_1 = \frac{L}{2\rho_{22}} \quad \dots (3.5)$$

Thus the locus of input port immittance for lossless load terminations is a circle with centre at  $(a_1, b_1)$  and radius  $c_1$ .<sup>25-27</sup> This is illustrated in Figure 3.1.

Similarly, the locus of output-port immittance,  $p_{out}$ , for lossless source terminations,  $j\sigma_s$ , is a circle defined by

$$(\rho_{out} - a_2)^2 + (\sigma_{out} - b_2)^2 = c_2^2 \quad \dots (3.6)$$

where  $a_2 = \rho_{22} - \frac{M}{2\rho_{11}}$ ,  $b_2 = \sigma_{22} - \frac{N}{2\rho_{11}}$  and  $c_2 = \frac{L}{2\rho_{11}}$ .  
 $\dots (3.7)$

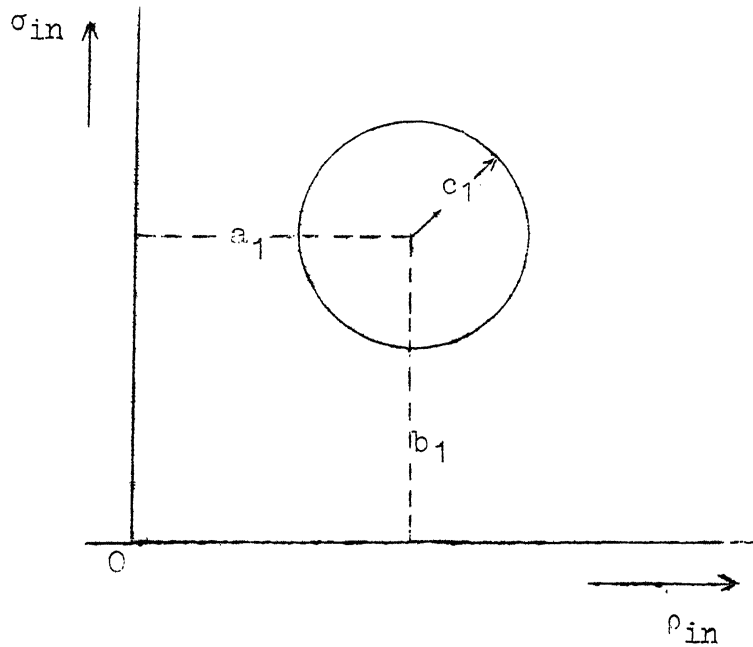


Fig. 3.1: Locus of  $p_{in}$  for reactive terminations,  $j\sigma_L$  at output-port.

These circles can be drawn by computing  $a_1$ ,  $b_1$  and  $c_1$  or  $a_2$ ,  $b_2$  and  $c_2$  from the matrix parameters of the two-port. Each circle can also be drawn from three measurements at one port with lossless terminations at opposite port.<sup>27</sup>

These circles hereafter would be referred as input reactance circle and output reactance circle, for convenience.

### 3.2.2 Driving Point Immittance of an Active Two-Port Terminated in a Real Immittance:

Consider the case where the two-port is terminated in a purely real (+ve or -ve) immittance,  $\rho_L$ , at its output port.

$$\text{Then } \rho_{in} = \rho_{11} - \frac{\rho_{12} \rho_{21}}{\rho_{22} + \rho_L} \quad \dots (3.8)$$

eliminating  $\rho_2 (= \rho_{22} + \rho_L)$  from  $\rho_{in}$  and  $\sigma_{in}$  one can obtain the relation

$$(\rho_{in} - A_1)^2 + (\sigma_{in} - B_1)^2 = C_1^2 \quad \dots (3.9)$$

$$\text{where } A_1 = \rho_{11} - \frac{N}{2\sigma_{22}}, \quad B_1 = \sigma_{11} + \frac{M}{2\sigma_{22}} \quad \text{and} \quad C_1 = \frac{L}{2\sigma_{22}}. \quad (3.10)$$

Thus the locus of input port immittance for purely real terminations is also a circle with centre at  $(A_1, B_1)$  and radius  $C_1$ .

Similarly, the locus of output port immittance for purely real source terminations is a circle defined by

$$(\rho_{out} - A_2)^2 + (\sigma_{out} - B_2)^2 = C_2^2 \quad \dots (3.11)$$

$$\text{where } A_2 = \rho_{22} - \frac{N}{2\sigma_{11}}, \quad B_2 = \sigma_{22} + \frac{M}{2\sigma_{11}} \quad \text{and} \quad C_2 = \frac{L}{2\sigma_{11}} \quad (3.12)$$

These circles hereafter would be referred as input resistance circle and output resistance circle, for convenience.

### 3.3 Output Port Termination for a Given Input Port Immittance:

The termination required at the output/input port for any immittance point on the input/output reactance/resistance circle can be evaluated analytically or geometrically. The procedure is out lined in the following sections.

#### 3.3.1 Termination Required at Output-Port for any Point on the Input Reactance Circle:

Knowing  $\rho_{11}$ ,  $\sigma_{11}$  it is possible to evaluate the output termination<sup>28</sup> for any given point  $(\rho_{in}, \sigma_{in})$  on the circle of Figure 3.1. Shift the origin, 0, to 0' whose coordinates are  $\rho_{11}$  and  $\sigma_{11}$  and draw a new set of axes parallel to the old set. Call the new coordinates  $\rho'_{in}$  and  $\sigma'_{in}$ . This is illustrated by Figure 3.2. The new coordinates of the centre, C', of this circle are  $-M/2\rho_{22}$  and  $-N/2\rho_{22}$ . As expected point  $(\rho_{11}, \sigma_{11})$  in old coordinates or new origin lies on the circle.

From Eqns. (3.2) and (3.3), we get

$$\frac{\sigma'_{in}}{\rho'_{in}} = \frac{\sigma_{in} - \sigma_{11}}{\rho_{in} - \rho_{11}} = \frac{N-M}{M+N} \frac{\frac{\sigma_2}{\rho_{22}}}{\frac{\sigma_2}{\rho_{22}}} \quad \dots (3.13)$$

$$\text{Hence } \frac{\sigma_2}{\rho_{22}} = \frac{\frac{N}{M} - \frac{\sigma'_{in}}{\rho_{in}}}{1 + \frac{N}{M} \cdot \frac{\sigma'_{in}}{\rho_{in}}} = \tan(\theta - \phi) \quad \dots (3.14)$$

$$\text{where } \tan \theta = \frac{-N/2\rho_{22}}{-M/2\rho_{22}} \quad \text{and} \quad \tan \phi = \frac{\sigma'_{in}}{\rho'_{in}} \quad \dots (3.15)$$

The angles  $\theta$  and  $\phi$  are with reference to  $\rho'_{in}$  axis and are indicated in Figure 3.2.

It is possible to evaluate  $\sigma'_{in}/\rho'_{in}$  for any point on this circle, provided  $\rho_{11}$  and  $\sigma_{11}$  or the new origin  $O'$  known.  $N/M$  can be evaluated either from the four-pole parameters of the two-port or by measuring  $\rho'_{in}$  for three convenient lossless terminations,  $j\sigma_L$ , at output-port including  $\sigma_L = 0$  or  $\infty$ . In the latter case, a circle can be circumscribed through these three points including  $O'$  and the coordinates of the centre  $C'$  determined in terms of the new axes. These are  $-M/2\rho_{22}$  and  $-N/2\rho_{22}$ . Thus  $N/M$  and hence  $\sigma_2/\rho_{22}$  can be calculated through Eqn. (3.14).

It is also possible to evaluate  $\sigma_2/\rho_{22}$  geometrically. Let  $X$  be any point on the circle of Figure 3.2 and  $YO'$  a diameter through  $O'$ . Then with proper sign  $\sigma_2/\rho_{22}$  equals  $XY/O'X$ .

The terminations for certain important points on this circle - redrawn in Fig. 3.3 - are tabulated together with their significance in Table 3.1.

Similar analysis can be carried out on the output reactance circle to obtain the input source termination required.

### 3.3.2 Termination Required at Output-Port for any Point on the Input Resistance Circle:

The termination required at output-port for any point on the input resistance circle can be evaluated from the equation

$$\frac{\rho_2}{\sigma_{22}} = \tan (\phi - \theta) \quad \dots (3.16)$$

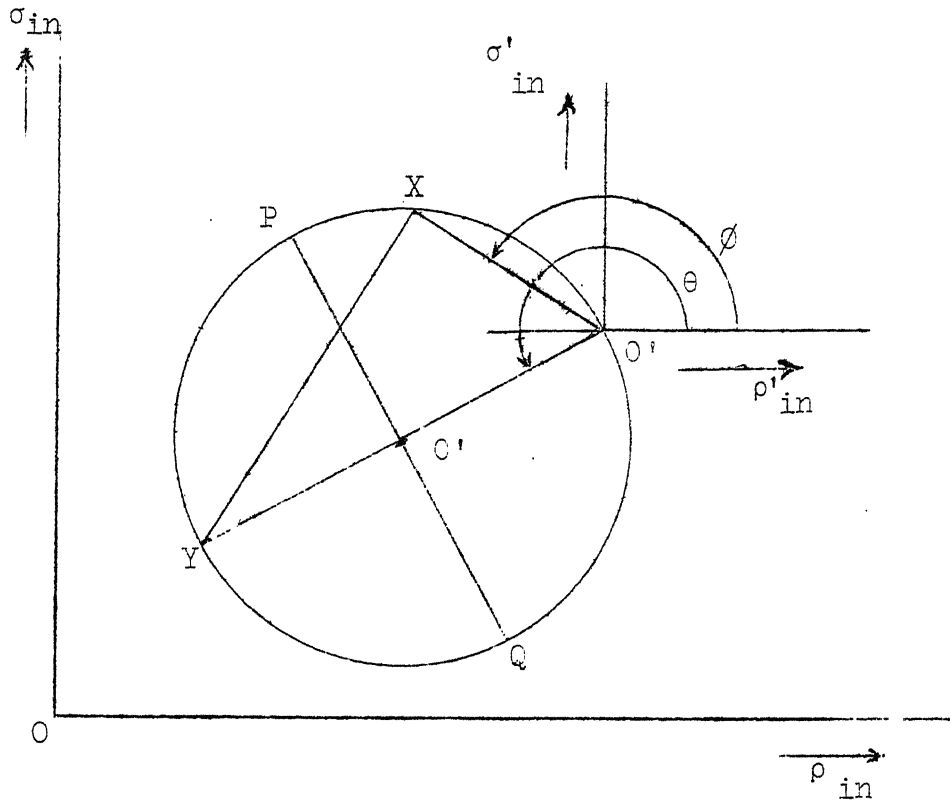


Fig. 3.2: Geometrical evaluation of  $\sigma_2/\rho_{22}$ .

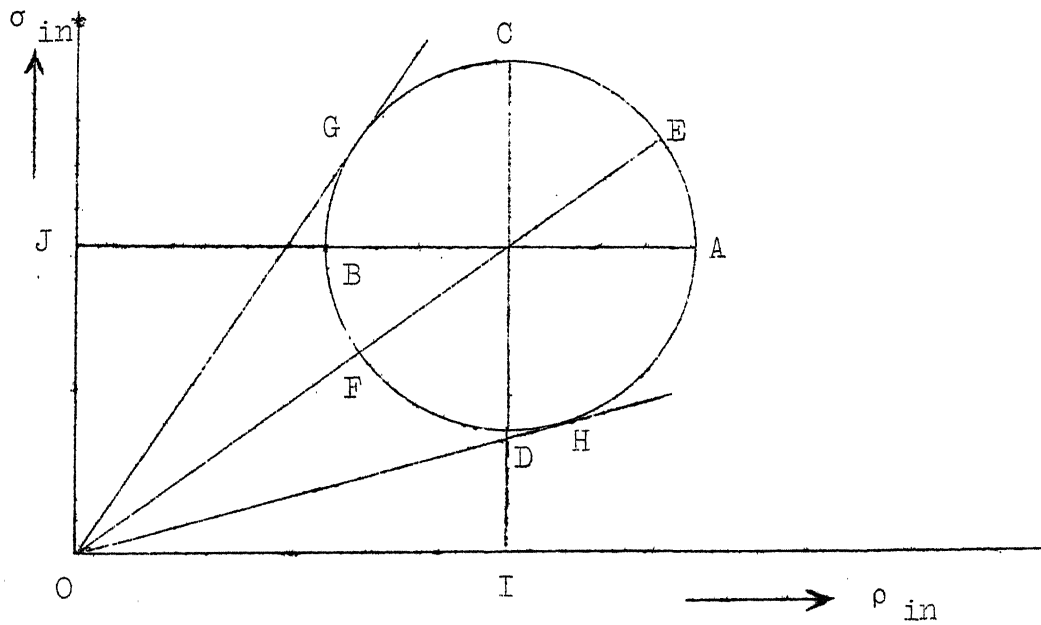


Fig. 3.3: Important points on the circle of input port immittance for which output terminations are calculated. OG and OH are tangents to the circle from the origin.

Table 3.1

Output termination for certain important points on the input reactance circle

Point on circle of $p_{in}$	$\rho_{11}$ and $\sigma_{11}$ are known		Significance
	$\rho_{in}$	$\sigma_{in}$	
		$\rho_{22}$ is known	
		$\sigma_2 / \rho_{22}$	
A	$a_1 + c_1$	$b_1$	$\rho_{in}$ maximum
B	$a_1 - c_1$	$b_1$	$\rho_{in}$ minimum
C	$a_1$	$b_1 + c_1$	$\sigma_{in}$ maximum
D	$a_1$	$b_1 - c_1$	$\sigma_{in}$ minimum
E	$a_1 \frac{(d_1 + c_1)}{d_1}$	$b_1 \frac{(d_1 + c_1)}{d_1}$	$ \rho_{in} $ maximum
F	$a_1 \frac{(d_1 - c_1)}{d_1}$	$b_1 \frac{(d_1 - c_1)}{d_1}$	$ \rho_{in} $ minimum
G	$e_1 \frac{(a_1 e_1 - b_1 c_1)}{d_1^2}$	$e_1 \frac{(b_1 e_1 + a_1 c_1)}{d_1^2}$	$\arg(p_{in})$ maximum
H	$e_1 \frac{(a_1 e_1 + b_1 c_1)}{d_1^2}$	$e_1 \frac{(b_1 e_1 - a_1 c_1)}{d_1^2}$	$\arg(p_{in})$ minimum

LEGEND:  $a_1 = \rho_{11} - \frac{M}{2\rho_{22}}$ ;  $b_1 = \sigma_{11} - \frac{N}{2\rho_{22}}$ ;  $c_1 = \frac{L}{2\rho_{22}}$ ;  $d_1 = (a_1^2 + b_1^2)^{\frac{1}{2}}$  and  $e_1 = (a_1^2 + b_1^2 - c_1^2)^{\frac{1}{2}}$

where

$$\tan \theta = \frac{\frac{M}{2\sigma_{22}}}{-\frac{N}{2\sigma_{22}}} \text{ and } \tan \phi = \frac{\sigma'_{in}}{\rho'_{in}} \quad \dots (3.17)$$

This equation can be derived from  $\rho_{in}$  and  $\sigma_{in}$  of  $p_{in}$  expression given in Eqn. 3.8.  $\rho_2$  can be evaluated analytically or geometrically by adopting the method explained in the above section. Table 3.2 summarizes the terminations required for certain important points on the circle.

#### 3.4 Axis of Skew Symmetry:

In Figure 3.2  $\sigma_2$  varies from 0 to  $\infty$  as we travel from Y to O' on the circumference of the circle. Point Y corresponds to tuning out of the port ( $\sigma_2 = 0$ ). Similarly, point O' corresponds to short circuit for h- and y- matrix environment. For g- and z-matrix environment the situation is reversed. Draw a line PQ perpendicular to YO' and passing through the centre C' as in Figure 3.2. For this case,  $\sigma_2/\rho_{22}$  at point P equals +1 and at point Q equals -1. It can be verified that the values of  $\sigma_2/\rho_{22}$  for any pair of points, one above and the other below the line YO' are equal in magnitude but opposite in sign. Hence the diameter YO' happens to be the axis of skew symmetry<sup>28</sup> with respect to phase of  $p_2$ .

Axis of skew symmetry can similarly be drawn for resistance circle. Point Y in this case, however, corresponds to tuning out of the port resistively ( $\rho_2 = 0$ ).

Table 3.2

Output termination for certain important points on the input resistance circle.

Point on circle $p_{in}$	$\rho_{11}$ and $\sigma_{11}$ are known		$\sigma_{22}$ is known	Significance
	$\rho_{in}$	$\sigma_{in}$	$\rho_2/\sigma_{22}$	
A	$A_1 + C_1$	$B_1$	$-(L + N)/M$	$\rho_{in}$ maximum
B	$A_1 - C_1$	$B_1$	$+(L - N)/M$	$\rho_{in}$ minimum
C	$A_1$	$B_1 + C_1$	$-(L - M)/N$	$\sigma_{in}$ maximum
D	$A_1$	$B_1 - C_1$	$+(L + M)/N$	$\sigma_{in}$ minimum
E	$\frac{A_1 (D_1 + C_1)}{D_1}$	$\frac{B_1 (D_1 + C_1)}{D_1}$	$-\frac{MA_1 + NB_1}{LD_1 + MB_1 - NA_1}$	$ p_{in} $ maximum
F	$\frac{A_1 (D_1 - C_1)}{D_1}$	$\frac{B_1 (D_1 - C_1)}{D_1}$	$-\frac{MA_1 + NB_1}{MB_1 - LD_1 - NA_1}$	$ p_{in} $ minimum
G	$\frac{E_1 (A_1 E_1 - B_1 C_1)}{D_1^2}$	$\frac{E_1 (B_1 E_1 + A_1 C_1)}{D_1^2}$	$-\frac{E_1 (NA_1 - MB_1) - C_1 (MA_1 + NB_1)}{LD_1^2 + C_1 (NA_1 - MB_1) + E_1 (NB_1 + MA_1)}$	$\arg (p_{in})$ maximum
H	$\frac{E_1 (A_1 E_1 + B_1 C_1)}{D_1^2}$	$\frac{E_1 (B_1 E_1 - A_1 C_1)}{D_1^2}$	$-\frac{E_1 (MB_1 - NA_1) - C_1 (MA_1 + NB_1)}{LD_1^2 + C_1 (NA_1 - MB_1) - E_1 (NB_1 + MA_1)}$	$\arg (p_{in})$ minimum

LEGEND:  $A_1 = \rho_{11} - \frac{N}{2\sigma_{22}}$  ;  $B_1 = \sigma_{11} + \frac{M}{2\sigma_{22}}$  ;  $C_1 = \frac{L}{2\sigma_{22}}$  ;  $D_1 = (A_1^2 + B_1^2)$  and  $E_1 = (A_1^2 + B_1^2 - C_1^2)$

LEGEND:  $A_1 = \rho_{11} - \frac{N}{2\sigma_{22}}$ ;  $B_1 = \sigma_{11} + \frac{M}{2\sigma_{22}}$ ;  $C_1 = \frac{L}{2\sigma_{22}}$ ;  $D_1 = (A_1^2 + B_1^2)^{1/2}$  and  $E_1 = (A_1^2 + B_1^2 - C_1^2)^{1/2}$

### 3.5 Sensitivity of Port Immittances:

#### 3.5.1 Sensitivity to Small Immittance Changes:

Define sensitivity<sup>29</sup>,  $K_{12}$  of total input port immittance,  $p_{p1}$ , for small immittance changes in the total output self-immittance,  $p_2$ , by

$$K_{12} = \frac{\frac{\partial (\ln p_{p1})}{\partial (\ln p_2)}}{\frac{\Delta p_{p1}}{p_{p1}}} = \frac{\Delta p_{p1}}{p_{p1}} \cdot \frac{p_2}{\Delta p_2} \quad \dots (3.18)$$

Similarly define sensitivity,  $K_{21}$  of total output port immittance,  $p_{p2}$ , for small immittance changes in the total input self immittance  $p_1$ .

From the above definitions

$$K_{12} = K_{21} = K = \frac{p_{12} p_{21}}{p_1 p_2 - p_{12} p_{21}} \quad \dots (3.19)$$

Thus the sensitivity,  $K$ , is an invariant for an interchange of input and output ports.

The modulus of sensitivity,  $|K|$ , is given by the expression

$$|K| = \frac{2}{\sqrt{\left\{ \left( \frac{2\rho_1\rho_2-M}{L} \right) - \left( \frac{2\sigma_1\sigma_2+M}{L} \right) \right\}^2 + \left\{ \left( \frac{2\rho_1\sigma_2-N}{L} \right) + \left( \frac{2\rho_2\sigma_1-N}{L} \right) \right\}^2}} \quad (3.20)$$

This expression can be rewritten as

$$|K| = \frac{2}{\sqrt{\left\{ \left( \frac{a'_1}{c'_1} - \frac{B'_1}{C'_1} \right)^2 + \left( \frac{A'_1}{C'_1} + \frac{b'_1}{c'_1} \right)^2 \right\}}} \quad \dots (3.21)$$

where  $a'_1, A'_1, b'_1, B'_1$  are the coordinates of centres and  $c'_1, C'_1$  radii of circles (including  $P_S, P_L$ ) defined by equations similar to Eqns.(3.5) and (3.10).

It is interesting to note that the factors

$$\frac{2^{\rho_1} \rho_2^{-M}}{L}, \quad \left| \frac{2^{\sigma_1} \sigma_2^{+M}}{L} \right|, \quad \left| \frac{2^{\rho_1} \sigma_2^{-N}}{L} \right| \text{ and } \left| \frac{2^{\rho_2} \sigma_1^{-N}}{L} \right|$$

are invariant in h-, z-, y- and g- matrix environments.

$$\text{i.e.} \quad \left| \frac{2^{\sigma_1} \sigma_2^{+M}}{L} \right|_h = \left| \frac{2^{\sigma_1} \sigma_2^{+M}}{L} \right|_y \text{ etc.} \quad \dots (3.22)$$

From Eqn. (3.19), the maximum modulus of sensitivity can be written as<sup>29</sup>

$$|K|_{\max} = \frac{L}{|p_1 p_2 - p_{12} p_{21}|_{\min}} \quad \dots (3.23)$$

since changes in  $p_S, p_L$  alter  $p_1, p_2$  but not the product  $p_{12} p_{21}$ .

From Eqn. (2.29)

$$\begin{aligned} |p_1 p_2 - p_{12} p_{21}|_{\min} &\geq |p_2|_{\min} |p_{p_1}|_{\min} \\ &\geq |p_1|_{\min} |p_{p_2}|_{\min} \end{aligned} \quad \dots (3.24)$$

The minimum of  $|p_2|$  and the minimum of  $|p_{p_1}|$  are usually obtained for different values of  $\sigma_2$ , the imaginary part of  $p_2$ . For the special case where these values coincide, the equality sign holds in statement (3.24). Similarly for the minimum of  $|p_1|$  and the minimum of  $|p_{p_2}|$ .

The minimum of  $|p_2|$  equals  $\rho_2$  and occurs when  $\sigma_2$  vanishes. The minimum modulus of  $p_{p_1}$  occurs when<sup>29</sup>

$$\sigma_1 = \frac{N}{2\rho_2} \quad \text{and} \quad \sigma_2 = \frac{N}{L+M} \cdot \rho_2 \quad \dots (3.25)$$

Thus

$$|p_{p_1}|_{\min} = \frac{2^{\rho_1} \rho_2 - M - L}{2\rho_2} \quad \dots (3.26)$$

Hence,

$$|K|_{\max} \leq \frac{1}{\delta}, \quad \text{where } \delta = \frac{\eta-1}{2} \quad \dots (3.27)$$

and hence  $\delta$  is an invariant in matrix environments or for immittance substitution, under arbitrary lossless terminations and for interchange of input and output ports.

### 3.5.2 Sensitivity Modulus Maximum:

Let the square of the modulus of the determinant,  $p_1 p_2 - p_{12} p_{21}$  be denoted by  $D$ . Thus

$$D = (\rho_1 \rho_2 - \sigma_1 \sigma_2 - M)^2 + (\rho_1 \sigma_2 + \rho_2 \sigma_1 - N)^2 \quad \dots (3.28)$$

$D$  is a maximum or minimum with respect to the variables  $\sigma_1$  and  $\sigma_2$  when Eqn. (2.27) is satisfied and  $\lambda = 0$ .

If  $p_{12} p_{21}$  is real and positive  $M = L$  and  $N = 0$ . Then, the only real root,  $\lambda_0$ , of Eqn. (2.27) equals zero. Then  $\sigma_1$  and  $\sigma_2$  both vanish. Hence Eqn. (3.28) gives

$$D_{\min} = (\rho_1 \rho_2 - M)^2 \quad \dots (3.29)$$

From Eqs. (3.19), (3.27) and (3.29)

$$|K|_{\max} = \frac{L}{\sqrt{D_{\min}}} = \frac{1}{\delta} \quad \dots (3.30)$$

because  $M = L$ .

The terminations  $\sigma_1$  and  $\sigma_2$  for this case can also be obtained from Eqn. (3.25) by substituting zero for  $N$ .

So far, we have considered the sensitivity for small immittance changes only. It is now proposed to investigate the sensitivity for large reactive changes.

### 3.5.3 Sensitivity to Large Reactive Changes:

Define an input sensitivity,  $K'_{12}$ , for large reactive changes at output port by<sup>29</sup>

$$K'_{12} = \frac{p'_{p_1} - p_{p_1}}{p_{p_1}} \cdot \frac{p_2}{p'_2 - p_2} = \frac{\Delta p_{p_1}}{p_{p_1}} \cdot \frac{p_2}{\Delta p_2} \quad \dots (3.31)$$

Here, the input port immittance has an initial value  $p_{p_1}$  and a final value  $p'_{p_1}$  due to a large reactive change in the output self immittance from  $p_2$  to  $p'_2$ . Thus Eqns. (3.18) and (3.31) are similar in form but not in detail; changes in Eqn. (3.18) refer to small immittances, whereas in Eqn. (3.31) large reactive changes are considered.

Similarly an output sensitivity,  $K'_{21}$ , for large reactive changes at input port can be defined.

$$\text{Now } |K'_{12}|_{\max} = \frac{L}{|p'_2 p_{p_1}|_{\min}} \quad \dots (3.32)$$

$|p_{p_1}|_{\min}$  is given by Eqn. (3.26) and occurs when condition (3.25) is satisfied.  $|p'_2|_{\min}$  occurs when the final value of the imaginary part of  $p_2$ , i.e.  $\sigma'_2$ , vanishes. Thus, as in Eqn. (3.25), the initial value of  $\sigma_2$  can be  $Np_2/(L+M)$  and its final value  $\sigma'_2$  can be zero so that

$$|K'_{12}|_{\max} = \frac{2L}{2\sigma_1 p_2 - M - L} = \frac{1}{\delta} \quad \dots (3.33)$$

Since  $\delta$  is reciprocal, it follows that

$$|K'_{12}|_{\max} = |K'_{21}|_{\max} = |K'|_{\max} \text{ say.}$$

Thus, the maximum modulus of the sensitivity of the total port immittance to large reactive changes of the total self immittance at the opposite port equals  $\delta$ .

Proceeding on similar lines it is possible to show that the maximum modulus of sensitivity, say  $|K''|$ , for large purely real (including -ve values) immittance variation is given by

$$|K''|_{\max} = \frac{2}{|\gamma - 1|} \quad \dots \quad (3.34)$$

where  $\gamma = \frac{2\sigma_1\sigma_2 + M}{L}$

### 3.6 Measurement of $\eta_i$ , Optimum Terminations and MAG:

The values of  $\eta$  and optimum terminations are simply related to the coordinates of centres and radii of input and output reactance circles.

From the expressions of  $a_1, b_1, c_1, a_2, b_2, c_2$  and  $\eta_i$  it can easily be shown that

$$\eta_i = \frac{a_1}{c_1} = \frac{a_2}{c_2} \quad \dots \quad (3.35)$$

The optimum source and load terminations are given by

$$\begin{aligned} \sigma_S &= - \left( \sigma_{11} - \frac{N}{2\rho_{22}} \right) = -b_1 \\ \rho_S &= \frac{L}{2\rho_{22}} \sqrt{(\eta_i^2 - 1)} = \sqrt{a_1^2 - c_1^2} \end{aligned} \quad \dots \quad (3.36)$$

$$\begin{aligned} \sigma_L &= - \left( \sigma_{22} - \frac{N}{2\rho_{11}} \right) = -b_2 \\ \text{and } \rho_L &= \frac{L}{2\rho_{11}} \sqrt{(\eta_i^2 - 1)} = \sqrt{a_2^2 - c_2^2} \end{aligned}$$

Knowing  $\left| \frac{p_{21}}{p_{12}} \right|$ , MAG can be computed from the relation

$$\text{MAG} = \frac{1}{s_i} \left| \frac{p_{21}}{p_{12}} \right| = \frac{1}{\eta_i + \sqrt{(\eta_i^2 - 1)}} \left| \frac{p_{21}}{p_{12}} \right|$$

For finding the measure of non-reciprocity the experimental method of Cripps and Slatter<sup>30</sup> can be adopted. If the two-port is terminated by convenient equal immittances,  $p_S, p_L$  in  $z$ -environment and moduli of forward and reverse operating voltage gains,  $g_{vf}, g_{vr}$  taken,

$$\left| \frac{p_{21}}{p_{12}} \right| = \frac{g_{vf}}{g_{vr}} \quad \dots \quad (3.37)$$

Thus from eight simple measurements<sup>27</sup>, three at the input port and three at the output port for plotting the circles and two more for evaluating the measure of non-reciprocity it is possible to evaluate  $\eta_i$  or  $s_i$ , optimum  $\rho_L, \sigma_L, \rho_S, \sigma_S$ , measure of non-reciprocity  $\left| \frac{p_{21}}{p_{12}} \right|$  and MAG.

The port immittance circle may lie in any part of the complex plane depending on the parameters of the two-port. By choosing proper feed back network and terminating immittance it is possible to realise the required driving point immittance.

Circuits for simulating inductance using transistor(s) and R-C elements are presented in the following chapters. Port immittance circles are used in the design of these circuits.

## CHAPTER IV

### INDUCTANCE SIMULATION - I

#### 4.1 Introduction:

The need of a high  $Q$  inductance for use in integrated circuits is recognised for some time. Aside from the endeavours to have an inductance in the form of an evaporated film, there have been many attempts to realise them by the use of active semiconductor devices. The later may be classified under two categories. One makes use of the reactance transistor circuit<sup>31-36</sup> and the other the inductive transistor circuit.<sup>37-47</sup>

The basic reactance transistor circuit<sup>31-33</sup> can realise large values of inductance but only of low  $Q$ . Jindal<sup>34</sup> has stated that a reactance transistor circuit can give inductive reactance with even infinite  $Q$ , when a resistance is added in series with base of the transistor.

In this chapter the reactance transistor circuit is analysed and a design procedure presented for realising the required inductance with maximum  $Q$  at the operating frequency. The analysis and design of Jindal's circuit for realising required inductance with infinite ' $Q$ ' is also presented. Examples based on a particular transistor are included. The design procedures are in terms of short circuit admittance matrix parameters and make use of the reactance circle.

Inductive transistor circuits are considered in the following chapter.

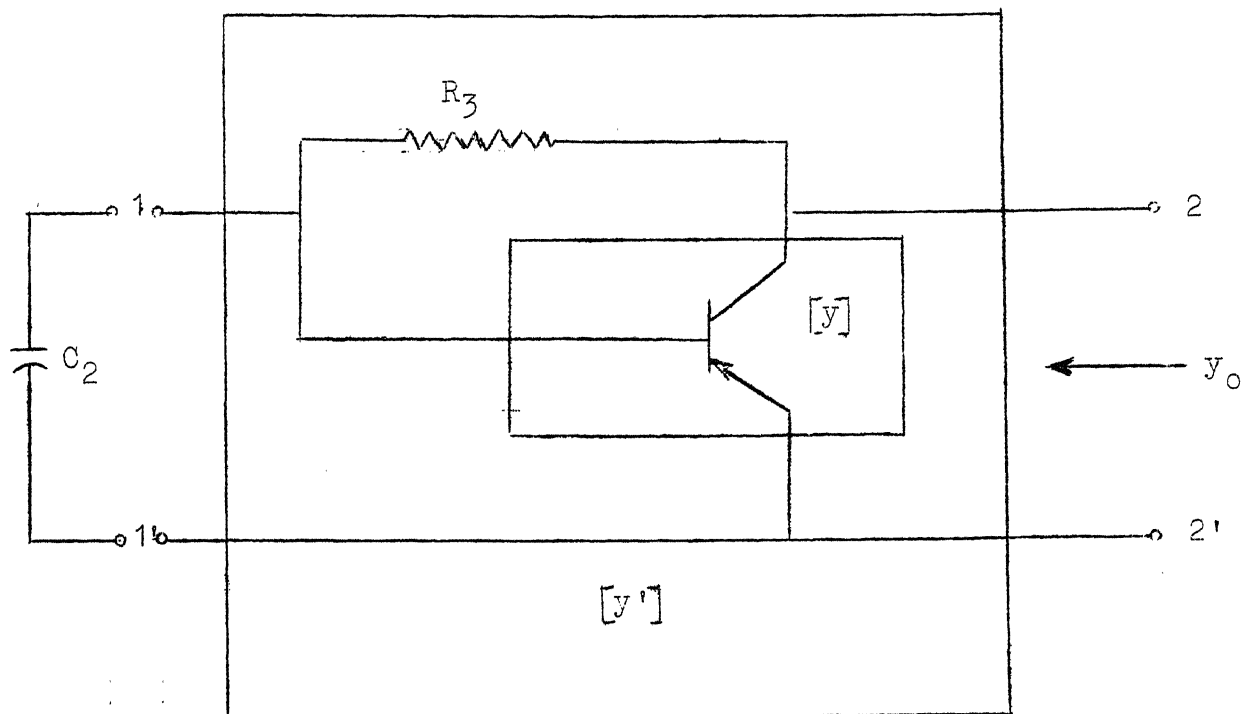
## 4.2 The Basic Reactance Transistor Circuit:

### 4.2.1 Basic Theory:

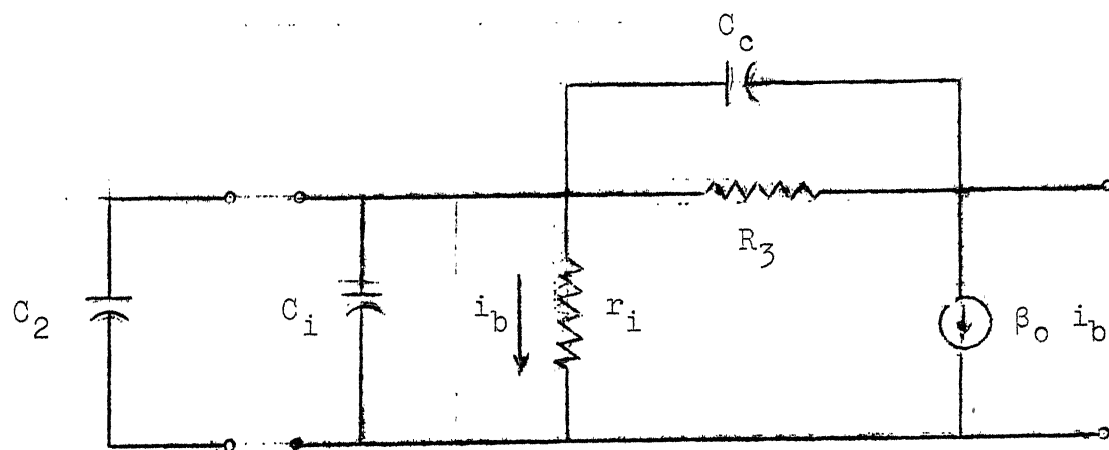
The basic reactance transistor circuit alongwith its equivalent circuit<sup>33</sup> is shown in Fig. 4.1. The components  $R_3$  and  $C_2$  are external to transistor. The base voltage of the transistor in Fig. 4.1(a) lags the collector voltage by almost  $90^\circ$ , if  $R_3 \gg 1/\omega C_2$  and the input impedance of the transistor is  $\gg 1/\omega C_2$ . The resulting collector current which is in phase with the base voltage lags the collector voltage by nearly  $90^\circ$ . Consequently, the circuit appears inductive to an external source. This can be established by analysing the equivalent circuit given in Fig. 4.1(b).

### 4.2.2 Analysis:

In Fig. 4.1(b)  $C_c$  is the collector diode capacitance but can include external collector base capacitance if the base spreading resistance,  $r_b \ll 1/\omega C_c$ . If the collector to base shunt diode conductance,  $g_c$ , is comparable to  $1/R_3$ , it should be added to  $1/R_3$ . Neglecting excess phase, the frequency response of the transistor can be approximated by the single pole model. This is done by letting  $1/r_i C_i = \omega_\beta$  in the equivalent circuit of Fig. 4.1(b), where  $\omega_\beta$  is the common emitter current gain cut-off frequency. The input resistance,  $r_i = r_e/(1-\alpha_o)$ , where  $r_e$  is the emitter resistance and  $\alpha_o$  is the common base low frequency current gain.



(a)



$$\beta_o = \alpha_o / (1 - \alpha_o)$$

(b)

Fig. 4.1(a) The reactance transistor  
 (b) Equivalent circuit for the reactance transistor.

If we now let  $\omega_\beta = (1 - \alpha_o) \omega_\alpha$ , then straight forward small signal analysis of the equivalent circuit of Fig. 4.1(b) yields<sup>33</sup> an expression for the equivalent series reactance

$$X = \left[ \frac{\omega}{\left\{ 1 + \left( \frac{\omega}{\omega_c} \right)^2 \right\} \left\{ 1 + \left( \frac{\omega}{\omega_\alpha} \right)^2 \right\}} \right] \left\{ \frac{(\alpha_o R_3 - r_e)}{\omega \frac{1}{\alpha}} - \frac{\alpha_o R_3}{\beta_o \omega_c} - \frac{\omega^2}{\omega_\alpha^2 \omega_c} \left( \frac{R_3}{\omega_\alpha^2} + \frac{r_e}{\omega_c} \right) \right\}$$

where  $\omega_c = \frac{1}{R_3 C_c}$ , and  $\frac{1}{\omega_\alpha^2} = \frac{1}{\omega_\alpha} + r_e C_2$  ... (4.1)

The equivalent series resistance of the circuit is

$$R = \left[ \frac{1}{\left\{ 1 + \left( \frac{\omega}{\omega_c} \right)^2 \right\} \left\{ 1 + \left( \frac{\omega}{\omega_\alpha} \right)^2 \right\}} \right] \left\{ r_e + \frac{\alpha_o R_3}{\beta_o} + \omega^2 \left( \frac{R_3}{\omega_\alpha^2} + \frac{\alpha_o R_3}{\omega_\alpha^2 \omega_c} + \frac{r_e}{\omega_c^2} \right) \right\} \dots (4.2)$$

From equation (4.1) we see that the circuit is certainly inductive if  $\beta_o \omega_c \gg \omega_\alpha^2$ . Because the minimum value  $C_c$  is fixed by the device, one must either make  $R_3$  small or  $C_2$  large in order to obtain inductance.

#### 4.2.3 Design Procedure:

The analysis of the circuit given above is very useful in understanding the circuit operation. But it is not useful in developing a design procedure. In many linear integrated circuit problems one is required to realise a specified value of inductance with a specified Q factor at an operating frequency. Hence, a design procedure in terms of the transistor

parameters at the operating frequency is developed below. The design developed is for maximum  $Q$  as the  $Q$  can always be lowered by shunting the inductance with a proper value of resistance.

The transistor in the common emitter configuration of Fig. 4.1(a) can be represented by its admittance matrix

$[y] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$ . The same with  $R_3$  included, can be represented by a modified admittance matrix

$$[y'] = \begin{bmatrix} y'_{11} & y'_{12} \\ y'_{21} & y'_{22} \end{bmatrix} \quad \dots \quad (4.3)$$

where

$$\begin{aligned} y'_{11} &= y_{11} + \frac{1}{R_3} & y'_{12} &= y_{12} - \frac{1}{R_3} \\ y'_{21} &= y_{21} - \frac{1}{R_3} & y'_{22} &= y_{22} + \frac{1}{R_3} \end{aligned} \quad \dots \quad (4.4)$$

$$\text{Let } y_{11} = g_{11} + jb_{11} \text{ etc, } y'_{11} = g'_{11} + jb'_{11} \text{ etc.} \quad (4.5)$$

$$y_{12} y_{21} = M + jN = L \angle \theta \quad \dots \quad (4.6)$$

$$\text{and } y'_{12} y'_{21} = M' + jN' = L' \angle \theta' \quad \dots \quad (4.7)$$

The locus of output admittance for susceptive input termination is a circle governed by the equation

$$\left( g_o - g'_{22} + \frac{M'}{2g'_{11}} \right)^2 + \left( b_o - b'_{22} + \frac{N'}{2g'_{11}} \right)^2 = \left( \frac{L'}{2g'_{11}} \right)^2 \quad \dots \quad (4.8)$$

This follows from Eqn. (3.6).

We are interested in realising an output port susceptance,  $jb_o$ , with maximum  $Q$  or minimum  $g_o$ . For a given  $b_o$  Eqn. (4.8)

can be rearranged in the form

$$A g_o^2 + B g_o + C = 0 \quad \dots \quad (4.9)$$

yielding

$$g_o = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \quad \dots \quad (4.10)$$

where

$$A = g'_{11} \quad \dots \quad (4.11)$$

$$B = M' - 2g'_{11}g'_{22} \quad \dots \quad (4.12)$$

$$C = g'_{11} g'^2_{22} + g'_{11} (b_o - b'_{22})^2 + (b_o - b'_{22}) N' - M' g'_{22} \quad (4.13)$$

From Eqns. (4.4) to (4.7)

$$\begin{aligned} g'_{11} &= g_{11} + g_3 & g'_{22} &= g_{22} + g_3 \\ b'_{11} &= b_{11} & b'_{22} &= b_{22} \\ M' &= M - g_3 (g_{12} + g_{21}) + g_3^2 & \dots & (4.14) \\ N' &= N - (b_{12} + b_{21}) g_3 \end{aligned}$$

where  $g_3 = 1/R_3$ .

A or  $g'_{11}$  ( $= g_{11} + 1/R_3$ ) is always positive for a short circuit stable network. Hence, for evaluating  $g_o$  minimum only the expression with -ve sign on the right hand side of Eqn. (4.10) need be considered.

For  $g_o$  to be minimum or maximum the differential of  $g_o$  w.r.t.  $R_3$ , the only variable in the expression for  $g_o$ , should be zero. This differentiation yields a sixth degree equation in  $R_3$ . This equation can be solved for positive real roots. The value of  $R_3$  giving the minimum value of  $g_o$  should be

selected from these roots. Value of  $C_2$  corresponding to this minimum  $g_o$  and specified  $jb_o$  can now be calculated from the equation

$$\frac{b'_{11} + b_S}{g'_{11}} = \frac{(g_o - g'_{22}) N' - (b_o - b'_{22}) M'}{(b_o - b'_{22}) N' + (g_o - g'_{22}) M'}$$

where  $b_S = \omega C_2$ . ... (4.15)

This follows from Eqn. (3.14).

Thus knowing the two-port parameters of the transistor it is possible to select the values of  $R_3$  and  $C_2$  to realise the required inductance with maximum 'Q'. Even the maximum Q realisable with this circuit is very low. This low 'Q' inductances, however, is useful in the design of wide band amplifiers.

#### 4.2.4 Example:

A transistor type AF 115 was chosen at  $I_e = 1$  mA,  $V_{ce} = -6$  V and  $T = 300^\circ$  K. Its common-emitter short circuited admittance parameters were measured at 5 MHz on an admittance bridge. Measured admittance parameters were as follows.

$$\begin{aligned} y_{11} &= 0.4 \text{ mS} & \text{and } + 65.0 \text{ pF} \\ y_{12} &= -2.5 \text{ pF} \\ y_{21} &= 35.4 \text{ mS} & \text{and } -169.4 \text{ pF} \\ \text{and } y_{22} &= 0.01 \text{ mS} & \text{and } + 3.0 \text{ pF.} \end{aligned}$$

The minimum value of inductance realised (for positive  $R_3$  and  $C_2$ ) with this transistor at 5 MHz was  $2 \mu\text{H}$ . The maximum Q obtainable is 3.06. The values of inductance, values of  $R_3$  and  $C_2$ , and the corresponding maximum Q realisable are summarized in Table 4.1.

Table 4.1

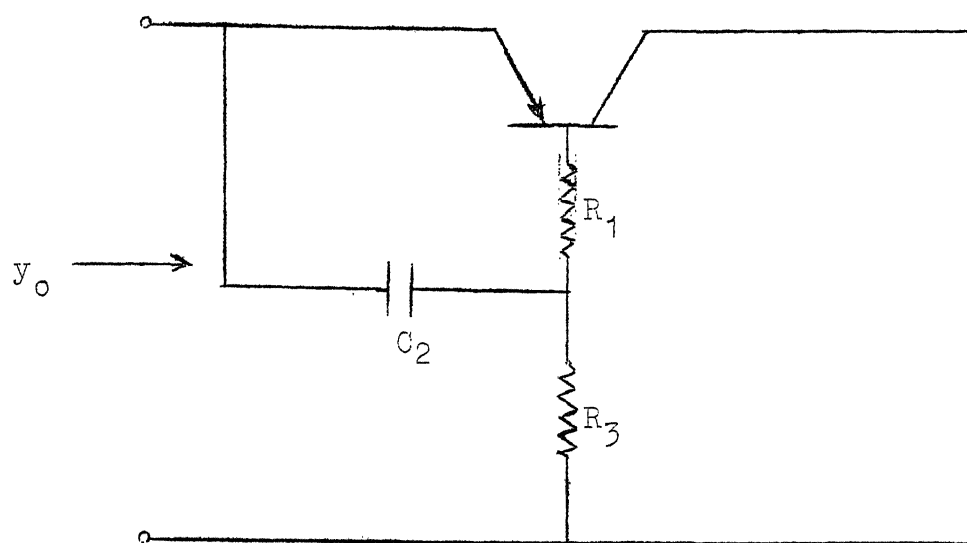
Values of  $R_3$  and  $C_2$  to realise given inductance with

Inductance ( $\mu\text{H}$ )	maximum Q.		Maximum Q
	$R_3$ (Ohms)	$C_2$ (pF)	
2.	318	62	1.15
3	605	81	2.07
4	801	93	2.53
5	968	103	2.80
6	1118	113	2.96
7	1254	122	3.03
8	1380	130	3.06
9	1498	138	3.05
10	1609	145	3.02

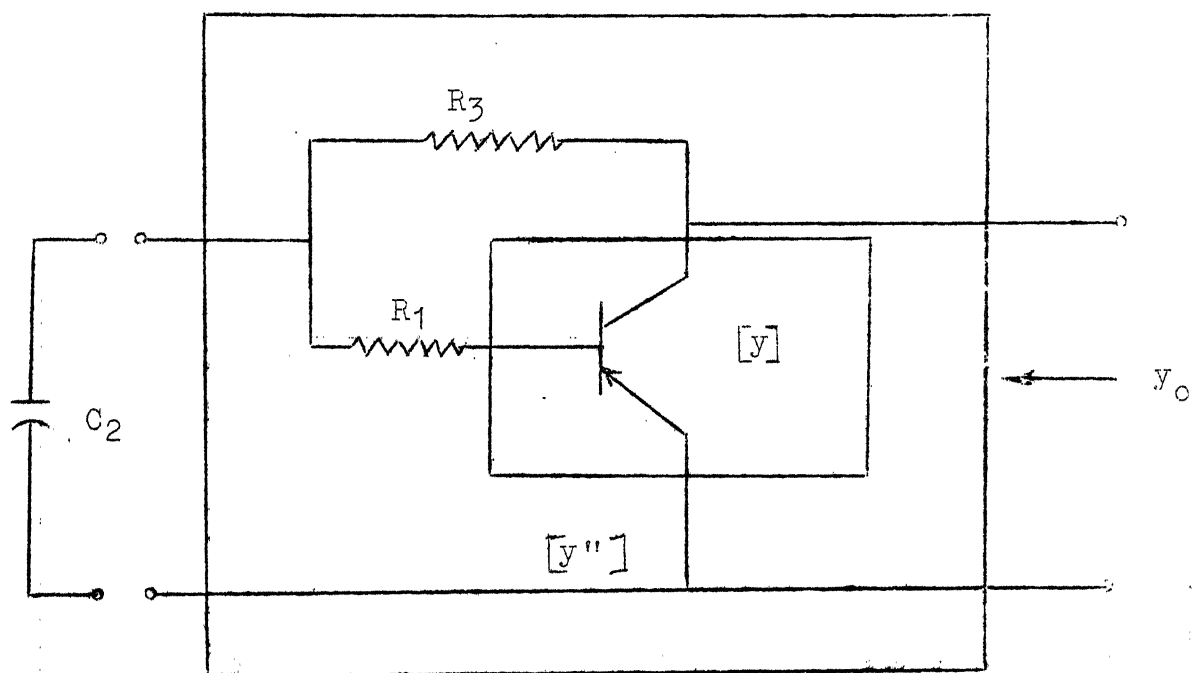
### 4.3 Modified Reactance Transistor Circuit:

#### 4.3.1 Theory:

Jindal<sup>34</sup> has stated that a circuit configuration represented in Fig. 4.2(a) can realise inductance with high or even infinite Q. Jindal's circuit can be rearranged as shown in Fig. 4.2(b). It can be observed that Jindal's circuit is similar to reactance transistor circuit of Fig. 4.1(a) with an extra resistance  $R_1$ , added in series with the base of the transistor. This  $R_1$  in conjunction with  $C_1$ , the input capacitance of the transistor produces extra lag in the collector current. This extra lag in collector current produces negative resistance and thus a high Q inductance across the output terminals.



(a)



(b)

Fig. 4.2(a) Jindal's circuit  
 (b) Modified reactance transistor circuit.

### 4.3.2 Analysis and Design:

The transistor in the common-emitter configuration of Fig. 4.2(b) can be represented by its admittance matrix

$$[y] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}. \quad \text{The same with } R_1 \text{ and } R_3 \text{ included, can be}$$

$$\text{represented by a modified admittance matrix } [y''] = \begin{bmatrix} y''_{11} & y''_{12} \\ y''_{21} & y''_{22} \end{bmatrix}$$

where

$$y''_{11} = \frac{1+y_{11}(R_1+R_3)}{R_3(1+y_{11}R_1)}, \quad y''_{12} = \frac{y_{12}R_3 - 1 - y_{11}R_1}{R_3(1+y_{11}R_1)}$$

$$y''_{21} = \frac{y_{21}R_3 - 1 - y_{11}R_1}{R_3(1+y_{11}R_1)}, \quad y''_{22} = \frac{1+y_{11}R_1+y_{22}R_3+R_1R_3\Delta}{R_3(1+y_{11}R_1)}$$

$$\dots \quad (4.16)$$

$$\text{and } \Delta = y_{11}y_{22} - y_{12}y_{21} = \Delta_r + j\Delta_i \quad \dots \quad (4.17)$$

$$\text{Let } y_{11} = g_{11} + jb_{11} \text{ etc, } y''_{11} = g''_{11} + jb''_{11} \text{ etc. } \dots \quad (4.18)$$

$$y_{12} + y_{21} = y_s = g_s + jb_s \quad \dots \quad (4.19)$$

$$y_{12}y_{21} = M + jN = L \angle \theta \quad \dots \quad (4.20)$$

$$\text{and } y''_{12}y''_{21} = M'' + jN'' = L'' \angle \theta \quad \dots \quad (4.21)$$

The stability based invariant factor,  $\eta$ , of the network with  $R_1$  and  $R_3$  is given by

$$\eta = \frac{2g''_{11}g''_{22} - M''}{L''} \quad \dots \quad (4.22)$$

The locus of output port admittance for susceptible input or generator termination,  $j b_s$ , is a circle with centre at

$$\left( \frac{2g''_{11}g''_{22} - M''}{2g''_{11}} \right), \left( \frac{2g''_{11}b''_{22} - N''}{2g''_{11}} \right) \text{ and of radius } \frac{L''}{2g''_{11}}.$$

When  $n$  equals unity, the output port admittance circle will just touch the  $j\omega$  axis and lie on its right. At the point of contact between this circle and the  $j\omega$  axis, the output port admittance,  $y_o$ , will be purely imaginary, being given by the ordinate of the centre of this circle. Thus at the point of contact

$$y_o = jb_o = j \left( \frac{2g_{11}'' b_{22}'' - N''}{2g_{11}''} \right) \quad \dots (4.23)$$

The  $Q$  corresponding to  $y_o$  of Eqn. (4.23) is infinite. The required input port susceptive termination,  $jb_s$ , for above  $y_o$ , is given by

$$\frac{b_{11}'' + b_s}{g_{11}''} = \frac{L'' - M''}{N''} \quad \dots (4.24)$$

Using Eqns. (4.16) to (4.21), Eqn. (4.23) can be rearranged<sup>35</sup> to express  $R_3$  in terms of  $R_1$ . The algebra is tedious. The final result is

$$R_3 = \frac{(A + BR_1 + CR_1^2)(1 + 2g_{11} R_1 + |y_{11}|^2 R_1^2)}{(D + ER_1 + FR_1^2 + GR_1^3)} \quad \dots (4.25)$$

Where

$$A = b_s + 2b_{22} - 2b_o \quad \dots (4.26)$$

$$B = 2(g_{11}b_{22} - g_{22}b_{11} + \Delta_i) + g_{11}b_s - g_sb_{11} - 4g_{11}b_o \quad \dots (4.27)$$

$$C = 2(g_{11}\Delta_i - b_{11}\Delta_r - b_o |y_{11}|^2) \quad \dots (4.28)$$

$$D = N - 2g_{11}(b_{22} - b_o) \quad \dots (4.29)$$

$$E = 2 \left\{ (Ng_{11} - Mb_{11}) - g_{11}(g_{11}b_{22} - g_{22}b_{11} + \Delta_i - 2b_o g_{11}) - (b_{22} - b_o)|y_{11}|^2 \right\} \quad \dots (4.30)$$

$$F = N(g_{11}^2 - b_{11}^2) - 2Mg_{11}b_{11} - 2g_{11}(g_{11}\Delta_i - b_{11}\Delta_r - b_o|y_{11}|^2) \\ - 2|y_{11}|^2(g_{11}b_{22} - g_{22}b_{11} + \Delta_i - 2b_o g_{11}) \quad \dots (4.31)$$

and

$$G = -2|y_{11}|^2 (g_{11}\Delta_i - b_{11}\Delta_r - b_o|y_{11}|^2) \quad \dots (4.32)$$

When the value of  $R_3$  as given by Eqns. (4.25) to (4.32) is substituted in  $n$  of Eqn. (4.22) taken as unity - for infinite  $Q$  - a 12th degree equation in  $R_1$  results. This equation has to be solved for positive real roots. Let the positive real roots of this equation be  $R_{1a}$ ,  $R_{1b}$  etc. Substitution of these values of  $R_1$  in Eqn. (4.25) gives real  $R_{3a}$ ,  $R_{3b}$  etc. Substitution of  $R_{1a}$  and  $R_{3a}$  in Eqn. (4.24) gives  $b_{Sa}$ . Similarly  $R_{1b}$ ,  $R_{3b}$  give  $b_{Sb}$ . It is then necessary to select a set of values like  $R_{1a}$ ,  $R_{3a}$ ,  $b_{Sa}$  such that  $R_{3a}$  and  $b_{Sa}$  are both positive.  $b_{Sa} = \omega C_{2a} R_{1a}$  is already positive. Only then, positive values for  $R_1$ ,  $C_2$  and  $R_3$  will be obtained. There can be more than one set of suitable values for  $R_1$ ,  $C_2$  and  $R_3$ . Any suitable set of values will give the desired inductance  $b_o$  with infinite  $Q$ .

#### 4.3.3 Example:

The same transistor type AF 115 described in Section 4.2.4 is chosen again for realising infinite  $Q$  inductance.

The maximum and minimum values of inductance realised with this transistor at 5 MHz were  $13\mu$  H and  $6\mu$  H respectively. The 12th degree equation in  $R_1$  yielded only two positive real roots  $R_{1a}$  and  $R_{1b}$  ( $R_{1b} > R_{1a}$ ). Eqn. (4.25) then gave two corresponding values  $R_{3a}$  and  $R_{3b}$  that were real and positive,

( $R_{3b} < R_{3a}$ ). Substitution in Eqn. (4.24) then gave two positive real values  $C_{2a}$  and  $C_{2b}$  ( $C_{2b} < C_{2a}$ ). Table 4.2 summarizes these results obtained with the help of a digital computer.

Values of inductance greater than  $13 \mu H$  upto  $40 \mu H$  with infinite  $Q$  were obtained by the addition of suitable values of capacitance  $C_4$  between base and emitter terminals. The problem is equivalent to changing  $b_{11}$  or base capacitance of the transistor and the same design procedure holds good for each value of  $C_4$ . Table 4.3 summarizes the effect of  $C_4$  on the maximum value of inductance realisable. Further increase in simulated inductance is possible with higher emitter currents.

These results are experimentally verified. For example, for inductance =  $10 \mu H$ , the output port  $Q$  was too high to be measured and the admittance bridge gave  $-98 pF$  at  $5 MHz$  instead of  $-100 pF$  which corresponds to  $10 \mu H$ . Where tolerance of components makes  $\eta$  of network slightly less than unity, the network can be brought to the verge of stability by a slight change in  $C_2$ , which does not affect inductance value. This follows from the property of the output port admittance circle.

Table 4.2

Two suitable sets of values for  $R_1, C_2$  and  $R_3$  to realise  
given  $L_o$  with infinite  $Q$

$L_o$ $\mu H$	$R_{1a}$ ohms	$C_{2a}$ pF	$R_{3a}$ ohms	$R_{1b}$ ohms	$C_{2b}$ pF	$R_{3b}$ ohms
6	577	163.2	466	744	155.8	392
7	444	148.7	711	1127	122.6	387
8	422	133.1	923	1394	100.7	437
9	430	118.7	1137	1622	83.9	514
10	461	104.8	1358	1816	70.4	621
11	516	91.2	1587	1963	59.3	771
12	612	77.0	1822	2033	50.1	991
13	803	61.1	2039	1944	42.9	1345

Table 4.3

Effect of capacitance  $C_4$  on the value of inductance

$$I_E = 1 \text{ ma. } C_{11} = 65.0 \text{ pF}$$

Capacitance $C_{11} + C_4$ pF	Minimum $L_o \mu H$	Maximum $L_o \mu H$
100	6	21
150	7	30
200	9	35
250	12	37
300	18	32

## CHAPTER 5

### INDUCTANCE SIMULATION - II

#### 5.1 Introduction:

A single non avalanche transistor with a resistance in the base can realize an inductance with low  $Q$ .<sup>32,37-43</sup> This circuit is referred as 'inductive transistor circuit'<sup>32,41</sup> in literature. Dutta Roy<sup>44</sup> reported a two transistor circuit which can realize high or even infinite  $Q$ , inductance. In this chapter the inductive transistor circuit and Dutta Roy's circuit are analysed. A design procedure for Dutta Roy's circuit is presented for realizing required inductance with infinite  $Q$ . It is in terms of short circuit admittance matrix parameters. An alternative circuit arrangement employing reactance transistor circuit is suggested. An illustrative example is included.

#### 5.2 Inductive Transistor Circuit:

A transistor with a grounded collector and a large base resistance may exhibit an inductance between emitter and ground if operated well above  $\beta$  and below  $\alpha$ -cut-off frequencies. The basic inductive transistor circuit alongwith its equivalent circuit is given in Fig. 5.1.

The input impedance of the inductive transistor circuit can be derived with the help of the equivalent circuit<sup>32</sup> given in Figure 5.1(b). If we assume that the collector cut-off :

frequency  $f_o = \frac{1}{2\pi R_b C_c}$ , is much higher than the alpha cut-off frequency  $f_\alpha$ , we get

$$Z_{in} = r_e + R_b (1-\alpha) \quad \dots (5.1)$$

The nature of variation of current amplification factor<sup>40</sup>,  $\alpha$ , for transistors is shown in Figure 5.2.  $\alpha$  in the base cut off region is approximately determined by the equation

$$\alpha = \frac{\alpha_o}{1+j \left(\frac{f}{f_\alpha}\right)} = \alpha_r - j \alpha_i \quad \dots (5.2)$$

Substituting for  $\alpha$  in equation (5.1)

$$Z_{in} = r_e + R_b (1-\alpha_r) + j R_b \alpha_i \quad \dots (5.3)$$

Thus  $R_b$  produces inductive part in the input impedance, provided the transistor is operated in the proper frequency range.

The inductive transistor of Figure 5.1(a) can be rearranged as shown in Figure 5.1(c).

The latter arrangement can be viewed as an active two-port terminated in a resistance at the input port. Knowing a set of matrix parameters for the active two-port the output port impedance circle for resistive termination at the input port may be plotted as explained in section 3.2.2 of Chapter 3. The maximum inductance, minimum inductance, maximum Q etc. realisable from this simple circuit and the corresponding resistive terminations required may now be evaluated analytically from the formulae given in Table 3.2 or geometrically from the circle plot as explained in section 3.3.2 of Chapter 3.

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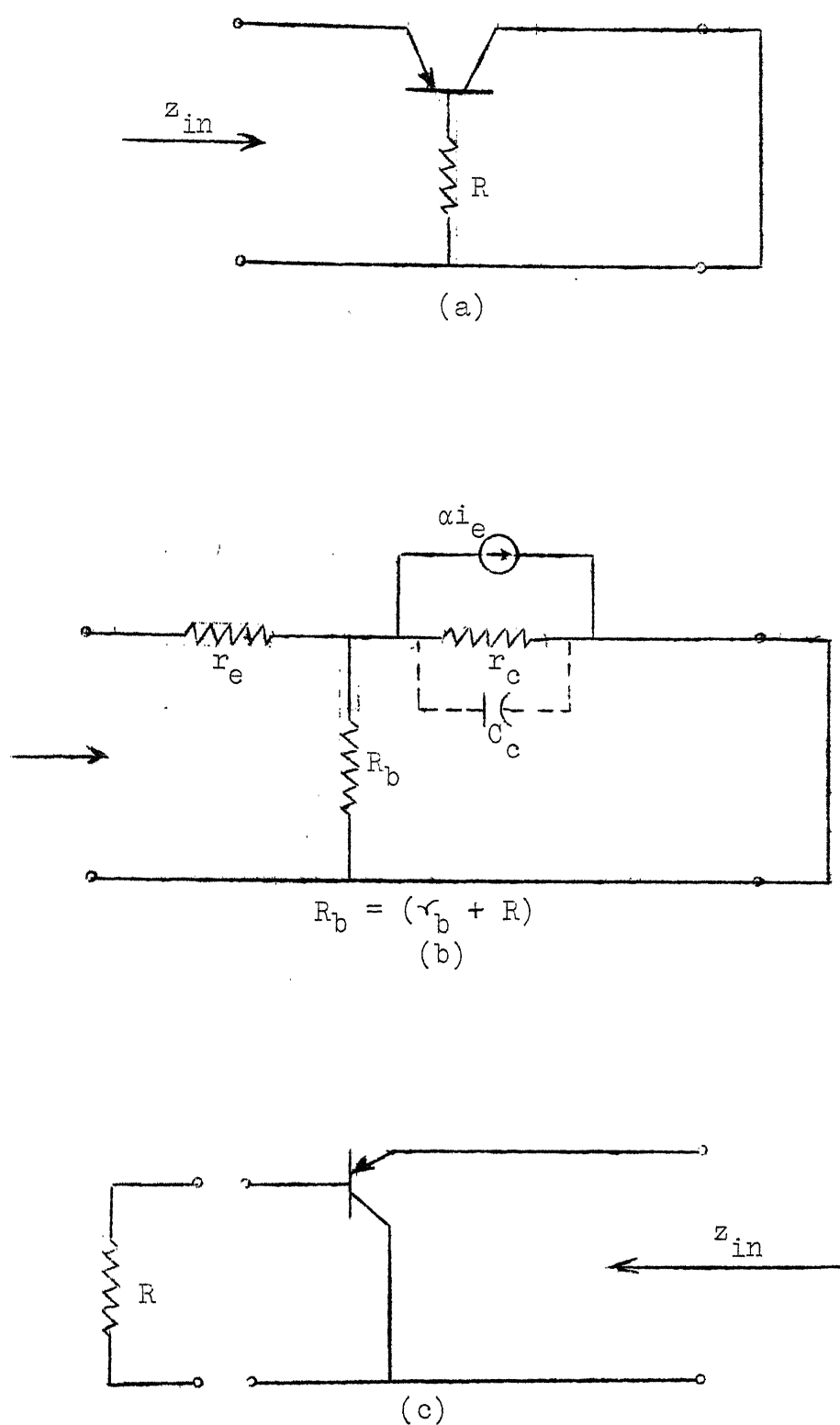


Fig. 5.1(a) The basic inductive transistor circuit  
 (b) Equivalent circuit of inductive transistor circuit  
 (c) Inductive transistor circuit rearranged

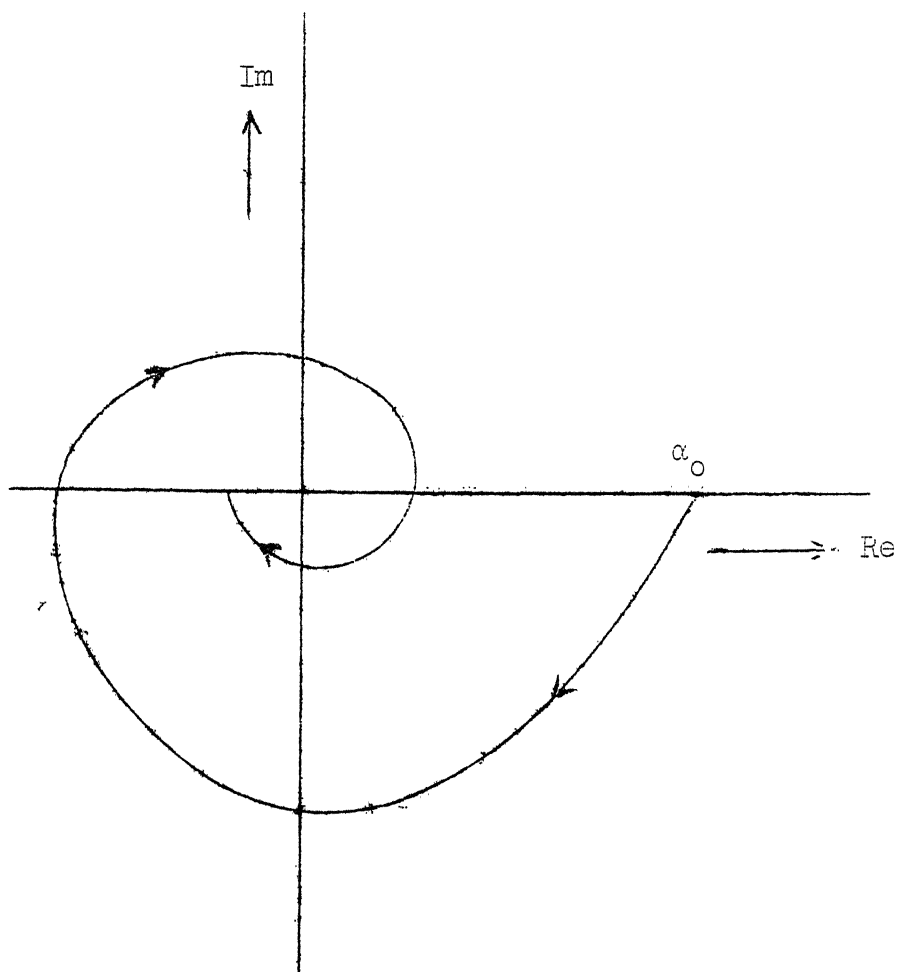


Fig. 5.2: Variation of ' $\alpha$ ' with frequency. Arrow indicates the direction for increase of frequency.

### 5.3 Dutta Roy's Circuit:

#### 5.3.1 Theory:

The circuit arrangement for realising high-Q inductance proposed by Dutta Roy<sup>44</sup> is shown in Fig. 5.3(a). This may be looked upon as an inductive transistor  $T_1$  connected at the base of another transistor  $T_2$ . The inductive transistor  $T_1$  can be replaced by its equivalent - lossy inductance - as shown in Figure 5.3(b). The input impedance,  $z'_{in}$ , of the composite transistor is given by

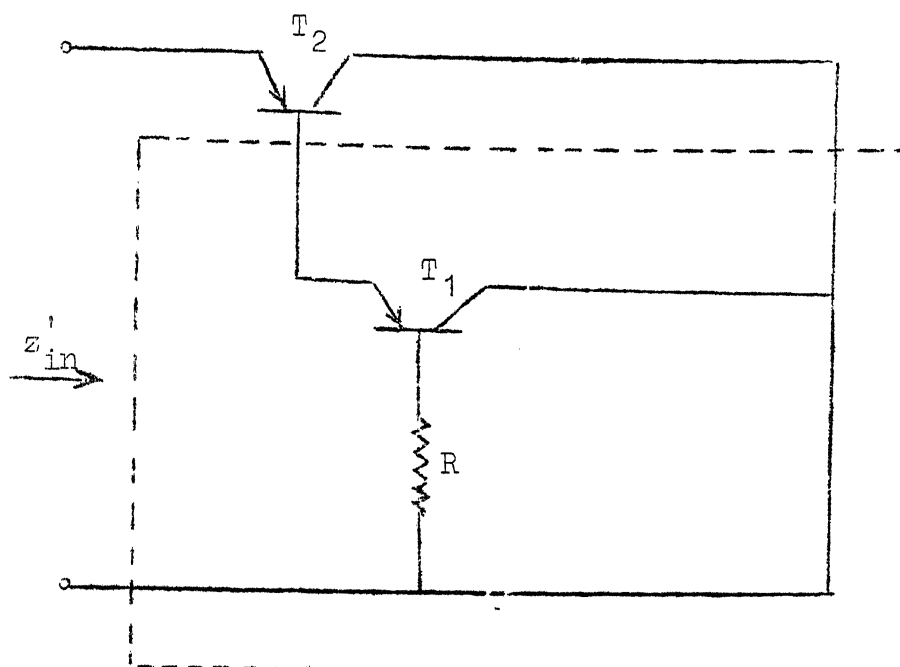
$$\begin{aligned} z'_{in} &= r'_e + [(R_1 + r'_b) + j X_1] [(1 - \alpha'_r) + j \alpha'_i] \\ &= [r'_e + (R_1 + r'_b)(1 - \alpha'_r) - \alpha'_i X_1] \\ &\quad + j [(1 - \alpha'_r) X_1 + \alpha'_i (R_1 + r'_b)] \quad \dots (5.4) \end{aligned}$$

where primed quantities refer to transistor  $T_2$ .

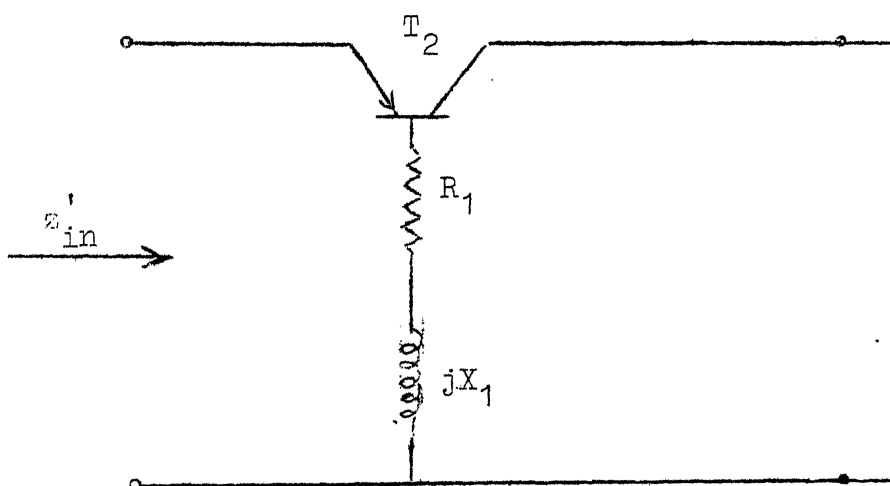
Thus by choosing proper frequency and proper  $X_1$  it is possible to reduce the resistive part to zero or even to -ve value and thus increase the 'Q'.

#### 5.3.2 Analysis and Design:

Rearrange<sup>47</sup> Dutta Roy's circuit as a cascaded two-port of two common collector amplifiers terminated by a source conductance  $g_S$  as shown in Figure 5.4. Transistor  $T_1$  (includes bias resistances  $R_1, R_2$ ) has a source admittance  $g_S$  while transistor  $T_2$  (includes bias resistances  $R_3, R_4$ ) sees a simulated source admittance  $g + g'_o + j b'_o$ .  $g'_o$  and  $b'_o$  are the real and imaginary parts of



(a)



(b)

Fig.5.3(a) Dutta Roy's circuit (b) Dutta Roy's circuit with the inductive transistor replaced by its equivalent 'lossy inductance'.

output admittance of transistor  $T_1$  terminated in  $g_S$ . For positive  $g$  and  $g_S$ , the simulated source admittance for transistor  $T_2$  ( $y'_S = g + g'_0 + j b'_0$ ) is equivalent to a low  $Q$  inductance. This makes the total self input admittance,  $y_1$  ( $= y_{11} + y'_S$ ) of transistor  $T_2$  satisfy the conditions

$$\begin{aligned} b_1 &= \text{Im}(y_1) < b_{11} \\ \text{and } g_1 &= \text{Re}(y_1) > g_{11} \end{aligned} \quad \dots (5.5)$$

Hence the output port admittance,  $y_o$ , of transistor  $T_2$  changes due to this simulated low  $Q$  inductance at its input port.

The 'output resistance circle' for transistor  $T_2$  is governed by the equation

$$(g_o - g_{22} + \frac{M}{2b_{11}})^2 + (b_o - b_{22} - \frac{M}{2b_{11}})^2 = (\frac{L}{2b_{11}})^2 \quad \dots (5.6)$$

The centre of this 'output resistance circle' moves from  $C$  to  $C'$  along  $AC$  when the transistor  $T_2$  is terminated by  $y'_S$ . Here  $A$  corresponds to  $g_{22} + jb_{22}$ . This is illustrated in Figure 5.5. The radius  $AC = \frac{L}{2b_{11}}$  while the changed radius  $AC' = \frac{L}{2b_1}$ . All data refer to transistor  $T_2$ .

The right choice of  $g_S$  and  $g$  makes the new circle cut/touch the imaginary axis at  $D$  where  $y_o = -j(OD) = -\frac{j}{\omega L_o}$ .  $O$  is the origin of coordinates,  $\omega$  the angular frequency considered and  $L_o$  the simulated inductance with infinite  $Q$ .

For any given  $b_o$  the termination,  $g_S$ , required may be evaluated from Eqn. (5.12).

Thus  $g_S$  can be chosen to provide the required inductance termination to transistor  $T_2$ .

If  $g_S$  is positive Eqn. (5.10) can be satisfied by adding a positive or negative conductance  $g$  at its input port. Provided  $g$  is also positive the required inductance with infinite  $Q$  is directly realizable. This procedure is illustrated by an example.

### 5.3.3 Example:

Two type 2N428 transistors were chosen to operate at  $I_e = 4\text{mA}$ ,  $V_{ce} = -4\text{V}$  and  $T = 300^\circ\text{K}$ . Their common collector  $y$ -matrix parameters were measured (alongwith their biasing resistances) at 5 MHz on an admittance bridge. Measured parameters for transistors  $T_1$  and  $T_2$  are given below.

Transistor  $T_1$ :

$$y_{11} = (9.10 + j 2.36) \text{ mS}$$

$$y_{12} = -(8.90 + j 2.23) \text{ mS}$$

$$y_{21} = -(8.74 - j 15.5) \text{ mS}$$

$$y_{22} = (9.64 - j 15.2) \text{ mS}$$

$$\text{Hence } y_{12}y_{21} = (112 - j 118) \mu\text{S}^2$$

Transistor  $T_2$ :

$$y_{11} = (9.05 + j 2.11) \text{ mS}$$

$$y_{12} = -(8.85 + j 1.95) \text{ mS}$$

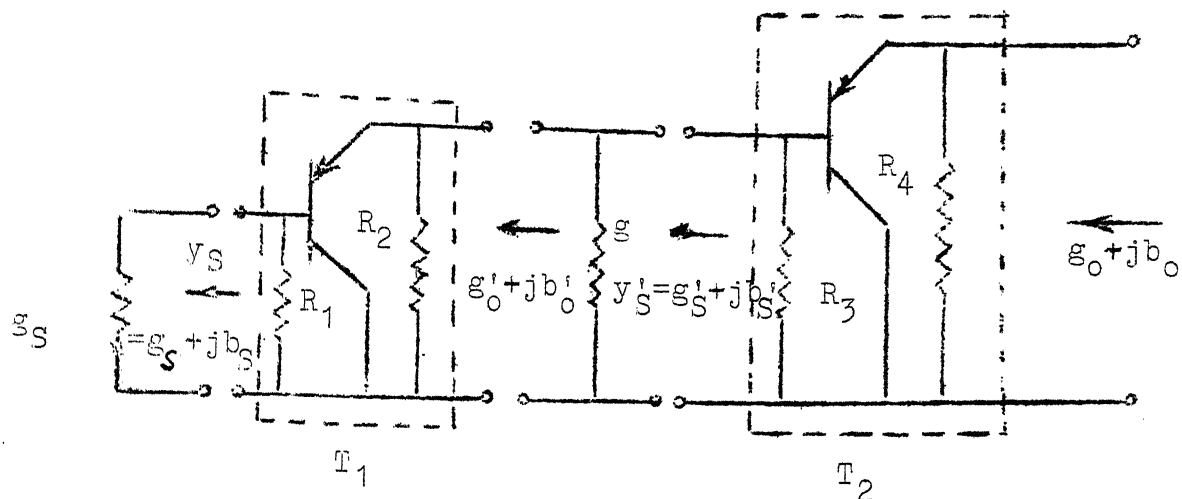


Fig. 5.4: A.C. equivalent of the circuit of Dutta Roy.  $R_1, R_2$  and  $R_3, R_4$  are biasing resistances of  $T_1$  and  $T_2$ . For the test circuit  $R_1$  and  $R_3$  each equals 5.1K in parallel with 56K while  $R_2$  and  $R_4$  each equals 10K.

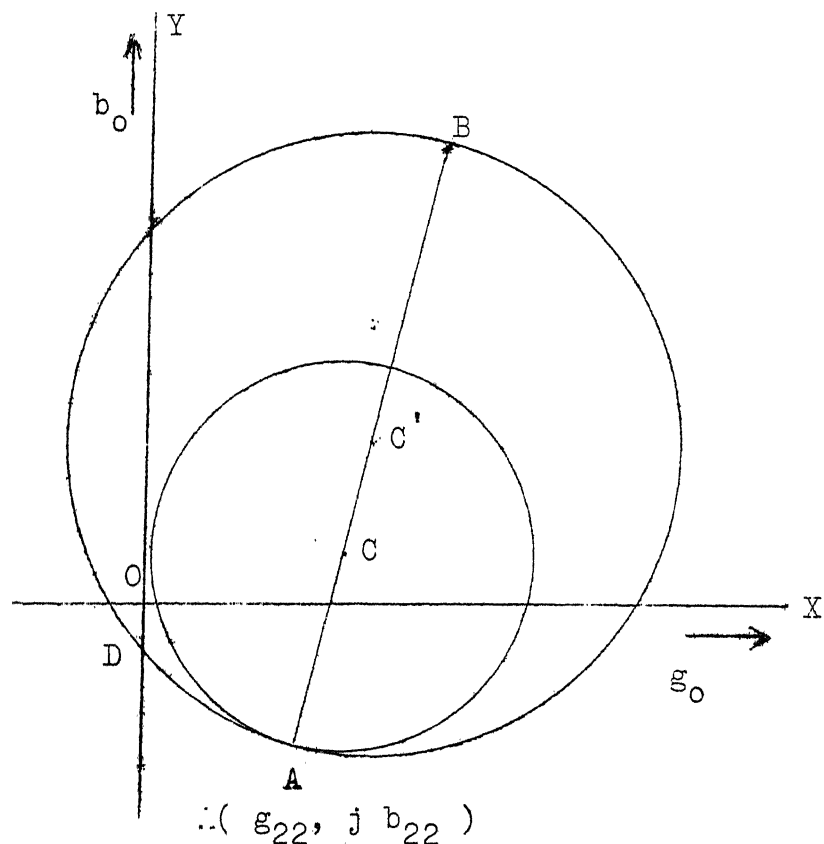


Fig. 5.5: Shifting of output port admittance circle of transistor  $T_2$  to realize point  $D = 0 - j \frac{1}{\omega L_0}$ , where  $L_0$  is the simulated inductance with infinite Q.

$$\begin{aligned}
 y_{21} &= -(10.7 - j 17.7) \text{ mS} \\
 y_{22} &= (11.6 - j 17.4) \text{ mS} \\
 \text{hence } y_{12}y_{21} &= (129 - j 136) \mu\text{S}^2
 \end{aligned}$$

Let a  $5 \mu\text{H}$  inductance with infinite  $Q$  be required at the output port of transistor  $T_2$ . At 5 MHz its susceptance  $b_o = -6.37 \text{ mS}$ . The susceptance needed at the input port of transistor  $T_2$  is calculated from Eqn. (5.9) and transistor  $T_2$  data. This susceptance,  $b'_S = b_1 - b_{11} = -2.73 \text{ mS}$ . To simulate  $b'_o = -2.73 \text{ mS}$  at the output port of transistor  $T_1$  we need a suitable source termination  $g_S$  which is given by Eqn. (5.12) and transistor  $T_1$  data,  $g_S = 1.80 \text{ mS}$ . Substituting for  $g_S$  in Eqn. (5.11) gives a simulated conductance  $g'_o = 2.06 \text{ mS}$ . Eqn. (5.10) with transistor  $T_2$  data,  $b_o = -\frac{1}{\omega L_o} = -6.37 \text{ mS}$ ,  $g_o = 0 \text{ mS}$  gives a  $g'_S$  of  $2.62 \text{ mS}$ . The extra conductance  $g$  required at the intermediate port equals  $(2.62 - 2.06) \text{ mS}$  or  $0.56 \text{ mS}$ .

Thus  $g_S$  at the input port equals  $1.80 \text{ mS}$  and  $g$  at the intermediate port equals  $0.56 \text{ mS}$ . At the output port an inductance of  $5 \mu\text{H}$  with infinite  $Q$  is obtained. These results have been verified experimentally.

#### 5.4 An Alternative Circuit Arrangement:

The inductive transistor circuit providing lossy inductance termination for transistor  $T_2$  in Fig. 5.4, may be replaced by a reactance transistor circuit as shown in Figure 5.6.

The inductance termination required at the input port of transistor  $T_2$  can be realised by adopting the design procedure

outlined in section 4.2.3 of Chapter 4. This circuit arrangement is more flexible than Dutta Roy's circuit as there is one more variable ' $C_2$ ' available for controlling the output port admittance of transistor  $T_1$ , which in turn controls the output port admittance

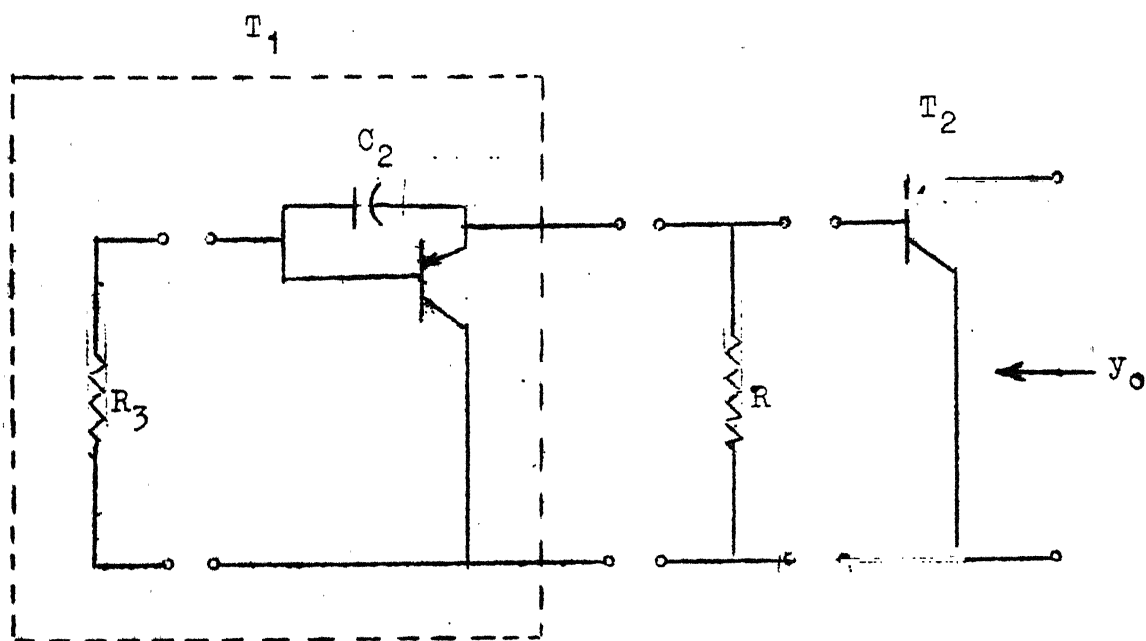


Fig. 5.6: An a.c. equivalent of the alternative circuit arrangement for realising high  $Q$  inductance.

of transistor  $T_2$ . This is confirmed by the results tabulated in Table 5.1. For the same value of simulated inductance, the reactive transistor  $T_1$  of Fig. 5.6 provides a higher  $Q$  than the inductive transistor  $T_1$  of Fig. 5.4.

Table 5.2 summarizes the values of components required for given output inductance with infinite  $Q$  for the circuit 5.4 of Dutta Roy employing an inductive transistor  $T_1$  and the modified circuit 5.6 employing a reactive transistor  $T_1$ . It can be seen that values of inductance beyond  $7\mu\text{H}$  upto  $9\mu\text{H}$  are obtainable only with the modified circuit of Fig. 5.6. The results are not very striking because transistor type 2N 428 used for simulating inductance at 5 MHz has a cut off of only 17 MHz.

When transistor type AF 115 with a cut off frequency of 75 MHz replaces transistor type 2N 428, the circuit of Dutta Roy does not realize an inductance with infinite  $Q$  of even  $1\mu\text{H}$  value. The modified circuit can realize upto  $7\mu\text{H}$ . The required values of components for realising various values of inductance are summarized in Table 5.3.

Table 5.1

Comparison of Q values of simulated inductance for inductive and reactive transistors

Output Inductance ( $\mu\text{H}$ )	Inductive transistor (2N 428*)		Reactive transistor (2N 428*)		
	Input port terminating resistance ( $\Omega$ )	Q of output inductance	Input port terminating resistance ( $\Omega$ )	Feedback capacitance (pF)	Q <sub>max</sub> of output inductance
3	54	1.78	Q <sub>max</sub> beyond	1.78	Requires negative capacitance
4	112	1.82	90	59	1.92
5	169	1.79	124	94	2.03+
6	225	1.73	156	117	2.09
7	282	1.66	187	133	2.10
8	339	1.58	217	144	2.07
9	395	1.51	246	153	2.03
10	452	1.44	274	161	1.97++
11	508	1.37	302	167	1.90
12	565	1.31	330	171	1.83
13	621	1.25	357	176	1.76
14	677	1.20	383	180	1.70
15	734	1.15	409	183	1.62

\*  $I_E = 4 \text{ mA}$ ,  $V_{CE} = -4 \text{ V}$ ,  $T = 300^\circ\text{K}$ , + Measured values  $L = 4.9 \mu\text{H}$ ,  $Q = 2.0$

++ Measured values  $L = 9.7 \mu\text{H}$ ,  $Q = 1.9$ .

Table 5.2

Values of components required for given output inductance with infinite Q for Dutta Roy's circuit and the modified circuit using transistor type 2N 428\*.

Output inductance ( $\mu\text{H}$ )	Dutta Roy's Circuit		Modified Circuit		
	Input port terminating resistance ( $\Omega$ )	Intermediate port terminating resistance ( $\Omega$ )	Input port terminating resistance ( $\Omega$ )	Feedback capacitance (pF)	Intermediate port terminating resistance ( $\Omega$ )
3	187	980	135	103	693
4	373	1.00 k	235	150	636
5	554	1.67 k	325	171	848 <sup>+</sup>
6	721	3.70 k	403	183	1.23 k
7	872	50.00 k	471	190	1.89 k
8	1.01k	-ve	530	196	3.27 k
9	1.13k	-ve	581	200	7.77 k <sup>++</sup>
10	1.24k	-ve	625	203	-ve

\*  $I_E = 4 \text{ mA}$ ,  $V_{CE} = -4 \text{ V}$  and  $T = 300^\circ\text{K}$ .

+ Measured values  $L = 4.9 \mu\text{H}$ ,  $Q = \text{very high}$  and not possible to measure.

++ Measured values  $L = 8.7 \mu\text{H}$ ,  $Q = \text{very high}$  and not possible to measure.

Table 5.3

Values of components required for given output inductance with infinite  $Q$  for the modified circuit using transistor type AF 115\*.

Output inductance ( $\mu\text{H}$ )	Input port terminating resistance ( $\Omega$ )	Feedback capacitance (pF)	Intermediate port terminating resistance ( $\Omega$ )
1	2.98 k	244	2.86 k
2	4.52 k	362	2.94 k
3	5.71 k	454	4.51 k
4	6.52 k	517	7.31 k
5	7.09 k	560	12.8 k
6	7.48 k	590	28.0 k
7	7.77 k	612	248 k

Not realisable beyond as intermediate port terminating resistance becomes negative

\*  $I_E = 1 \text{ mA}$ ,  $V_{CE} = -6\text{V}$  and  $T = 300^\circ\text{K}$ .

## CHAPTER 6

### CONCLUSIONS

Stability, power gain and sensitivity or the interaction between ports are simply related to the port immittance circles. Thus port immittance circles are useful in the study of basic properties of active two-ports.

The technique presented for the measurement of stability factor is very useful in the design of tuned amplifiers. The maximum modulus of sensitivity for small immittance changes and large reactive changes is also useful in the design of tuned amplifiers, as it specifies the interaction between ports while the tuning is carried out.<sup>29</sup>

Input/output port resistance/reactance circles can be drawn by measuring the input/output port immittance for three convenient resistance/reactance terminations at the opposite port. Drawing the port immittance circles for a three terminal device at its input and output ports, in all the three configurations, it is possible to know the potentialities of the device in realising driving point negative-resistance, inductance etc. The type of feed back component and the type of termination to be provided for realising required driving point immittance can also be inferred from these circles. For example, studies on transistor in its three configurations suggest - i) capacitive

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termination at input port reflects inductive reactance at output port in common emitter configuration. ii) resistive termination at input port in common collector configuration reflects inductive reactance at output port iii) inductance termination at input port in common collector configuration reflects inductive reactance and negative resistance at output port. Combination of (i) and (ii) yields the reactance transistor circuit, (ii) the inductive transistor circuit; and combination of (ii) and (iii) yields Dutta Roy's circuit.

The modified reactance transistor circuit of Jindal and the Darlington pair connection suggested by Dutta Roy can realise inductances with very high  $Q$ . For Dutta Roy's circuit the operating frequency should fall in the frequency band in which the transistor is potentially unstable in its common collector configuration. This restriction is not there for Jindal's circuit. Thus Jindal's circuit is less dependent on the device properties for its operation than Dutta Roy's circuit.

Both Jindal's and Dutta Roy's circuit configurations are sensitive to temperature<sup>34,46</sup>. This draw back, however, may be over come by the use of FETs which are less sensitive to temperature<sup>48</sup>.

The design procedures presented are completely general in terms of two-port matrix parameters. Hence, these procedures can be applied to design circuits for simulating inductances using FETs. Similar circuit configurations can be employed.

The recent trend is to simulate inductance by means of impedance convertors, gyrators<sup>49</sup> and unity gain amplifiers.<sup>50-51</sup> Excellent results have been reported. But the circuitry is rather complex.

## REFERENCES

1. LINVILL, J.G., "The relationship of transistor parameters to amplifier performance", IRE, AIEE Conference on transistor circuits, Pennsylvania University, February 17, 1955.
2. LLEWELLYN, F.B., "Some fundamental properties of transmission systems", Proc. IRE, Vol.40, No. 3, March 1952, pp. 271-283.
3. STERN, A.P., "Considerations on the stability of active elements and applications to transistors", IRE. Natl. Conv. Record, Pt. 2, 1956, pp. 46-52.
4. BAHRS, G.S., "Stable amplifiers using potentially unstable elements", IRE Wescon Conv. Record 1, Pt. 2, 1957, pp. 185-189.
5. GHAAUSI, M.S., "Principles and design of linear active circuits", McGraw Hill Book Co., 1965, pp. 62-69.
6. LINVILL, J.G. and GIBBONS, J.F., "Transistors and active circuits", McGraw Hill Book Co., 1961, Ch. 12.
7. GARTNER, W.W., "Transistors, principles, design and applications", D. Van Nostrand Co., 1960, pp.368-379.
8. PAGE, D.F. and BOOTHROYD, A.R., "Instability in two-port active networks", Trans. of IRE on circuit theory, Vol. CT-5, No.2, June 1958, pp. 133-139.
9. KUO, B.C., "Automatic control systems", Prentice Hall of India Pvt. Ltd., 1967, Ch. 7.
10. CHENG, C.C., "Neutralization and unilaterization", Trans. of IRE on circuit theory, Vol. CT-2, June 1955, pp.138-145.
11. STERN, A.P., ALDRIDGE, C.A., and CHOW, W.F., "Internal feedback and neutralisation of transistor amplifiers", Proc. IRE, Vol. 43, No. 7, July 1955, pp. 838-847.
12. CHU, G.Y., "Unilaterization of junction transistor amplifiers at high frequencies", Proc. IRE, Vol. 43, No. 8, August 1955, pp. 1001-1006.
13. COTE, A.J., Jr., "Evaluation of junction transistor neutralization networks", Trans. of IRE on circuit theory, Vol. CT-5, No. 2, June 1958, pp.95-103.

14. STERN, A.P., " Stability and power gain of tuned transistor amplifiers", Proc. IRE, Vol. 45, No. 3, March, 1957, pp. 335-343.
15. VENKATESWARAN, S. and BOOTHROYD, A.R., " Power gain and bandwidth of tuned transistor amplifier stages", Proc. IEE, Vol. 106, Pt. B, Suppl. No. 15, January 1960, pp. 518-529.
16. VENKATESWARAN, S. " An invariant stability factor and its physical significance", Proc. IEE, Vol. 109, Pt. C, No. 15, March 1962, pp. 98-102. (IEE Monograph No. 468E September 1961).
17. ROLLETT, J.M., " Stability and power gain invariants of linear two-ports", IRE Trans. on circuit theory, Vol. CT-9, No. 1, March 1962, pp. 29-32.
18. REFERENCE 6, pp. 242-248.
19. REFERENCE 5, pp. 70-72.
20. BRAMLEY, E.N., " Two-port terminations for maximum power gain", IRE, Trans. on circuit theory, Vol. CT-6, No. 4, December 1959, p. 390.
21. VENKATESWARAN, S. and SARMA, P.S., " Maximum available power gain of active two-ports", Electronics Letters, Vol. 4, No. 13, June 28, 1968, pp. 278-279.
22. VENKATESWARAN, S., " Stability, power gain and bandwidth of linear active four-pole networks, with particular reference to transistor amplifiers at higher frequencies", University of London Ph.D. Thesis, June 1961, Appendix 2.2, p. 92.
23. VAN VALKENBERG, M.E., " Modern Network synthesis", John Wiley and Sons, 1965, Ch. 16.
24. ZAWELS, J., " Travelling-wave analysis of generalised networks", IEE, Vol. 108, Pt. C, No. 14, September 1961, pp. 300-308.
25. ZAWELS, J., " Gain stability relationship", IEEE Trans. on circuit theory, " Vol. CT-10, No. 1, March 1963, pp. 109-110.
26. MEDINA, M.A. and SCARLETT, R.M., " A method of evaluating the stability factor of a two-port network", Proc. IEEE, Vol. 54, No. 12, December 1966, pp. 1959-60.

27. VENKATESWARAN, S. and SARMA, P.S., " Quick computation of stability factor, optimum terminations, and maximum power gain of active two-ports", Proc. IEE, Vol. 114, No. 11, November 1967, pp. 1655-1656.
28. SARMA, P.S. and VENKATESWARAN, S., " Port immittances of active two-port networks" - To be published in the inaugural issue of the Journal of Electronics and Data Processing, India.
29. VENKATESWARAN, S., " An invariant alignability factor and its significance", The Radio and Electronic Engineer, Vol. 35, No. 6, June 1968, pp. 361-368.
30. CRIPPS, L.G. and SLATTER, J.A.G., " Amplifier gain and stability", Jour. Brit. IRE, Vol. 22, No. 5, May 1961, p. 417.
31. FUJIMURA, Y. and MII, N., " Reactance transistor ", Proc. IRE, Vol. 48, No. 1, January 1960, p. 118.
32. DILL, H.G., " Inductive semiconductor elements and their application in band pass amplifiers", IRE Trans. on military electronics, Vol. MIL-5, No. 3, July 1961, pp. 239-250.
33. JOSEPHS, H.C., GEORGE, R.I. and BILLETTE, R., " Solid state inductors", Solid State Electronics, Vol. 8, No. 10, October 1965, pp. 775-788.
34. JINDAL, G.R., " A high Q single inductive transistor arrangement", Proc. IEEE, Vol. 55, No. 1, January 1967, pp. 105-107.
35. SARMA, P.S. and VENKATESWARAN, S., " Simulated inductance with a transistor and R-C elements", Electronics Letters, Vol. 5, No. 26, December 27, 1969, pp. 689-691.
36. VENKATESWARAN, S. and RADHAKRISHNA RAO, K., " Driving point inductance of a transistor with R-C feedback", Int. Journal of Electronics, Vol. 28, No. 4, April 1970, pp. 311-317.
37. EVANS, D.M., " Measurement on alloy type germanium transistors and their relation to theory ", Journal of Electronics, Vol. 1, No. 5, March 1956, pp. 461-476.
38. BURGESS, R.E., " Emitter base impedance of junction transistors", Journal of Electronics, Vol. 2, No. 3, November 1956, pp. 301-302.

- 39.. YAMAGUCHI, H., "On the inductive reactance and negative resistance in the transistor", Journal of Physical Society of Japan, Vol. 11, No. 6, June 1956, pp. 717-718.
- 40.. LINDMAYER, J. and WRIGLEY, C., "Some generalities of the transistor time mode for two-barrier devices", Journal of Electronics and Control, Vol. 13, No. 1, July 1962, pp. 137-158.
- 41.. DUTTA ROY, S.C., "The inductive transistor", IEEE Trans. Circuit theory, Vol. CT-10, No. 1, March 1963, pp. 113-115.
- 42.. LINDMAYER, J. and NORTH, W., "The inductive effects in transistors", Solid State Electronics, Vol. 8, No. 4, April 1965, pp. 409-415.
- 43.. ARCHER, J.A., GIBBONS, J.F. and PURNAYYA, G.M., "Use of transistor - simulated inductance as an interstage element in broadband amplifiers", IEEE Jour. of Solid-State Circuits, Vol. SC-3, No. 1, March 1968, pp. 12-21.
- 44.. DUTTA ROY, S.C., "A novel high Q inductance for micro-miniature circuits", Proc. IEEE, Vol. 52, No. 2, February 1964, pp. 214-215.
- 4-5.. SEN, S.K. and SEN, A.K., "Inductive behaviour of a transistor circuit comprising of n-transistors", Proc. IEEE, Vol. 54, No. 12, December 1966, pp. 1978-1979.
- 4-6.. SAITO, T., MIYAKAWA, T., IKEDA, T., TAHIRA, K. and ANDO, J., "A high Q temperature insensitive inductive transistor circuit", Solid State Electronics, Vol. 11, No. 5, May 1968, pp. 553-560.
- 4-7.. SARMA, P.S. and VENKATESWARAN, S., "High Q inductance from cascode transistor amplifier", Forthcoming in the Jour. of IEE and IRE, India.
- 4-8.. WEINBERG, Z. and BAR-LEV, A., "Inductance simulation using MOS transistors", Int. Journal of Electronics, Vol. 28, No. 6, June 1970, pp. 517-524.
- 4-9.. MITRA, S.K., "Analysis and synthesis of linear active networks", John Wiley and Sons, 1969, Chs. 9 and 10.
- 5-0.. DUTTA ROY, S.C., "Driving point function synthesis using a unity gain amplifier", IEEE Trans. on circuit theory, Vol. CT-17, No. 2, May 1970, pp. 266-268.
- 5-1.. RADHAKRISHNA RAO, K. and VENKATESWARAN, S., "High Q inductor from single unity gain amplifier", Int. Journal of Electronics, Vol. 29, No. 5, November 1970, pp. 485-489.

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